1,5 A, Step –Up/Down/luverting Switching Regulator

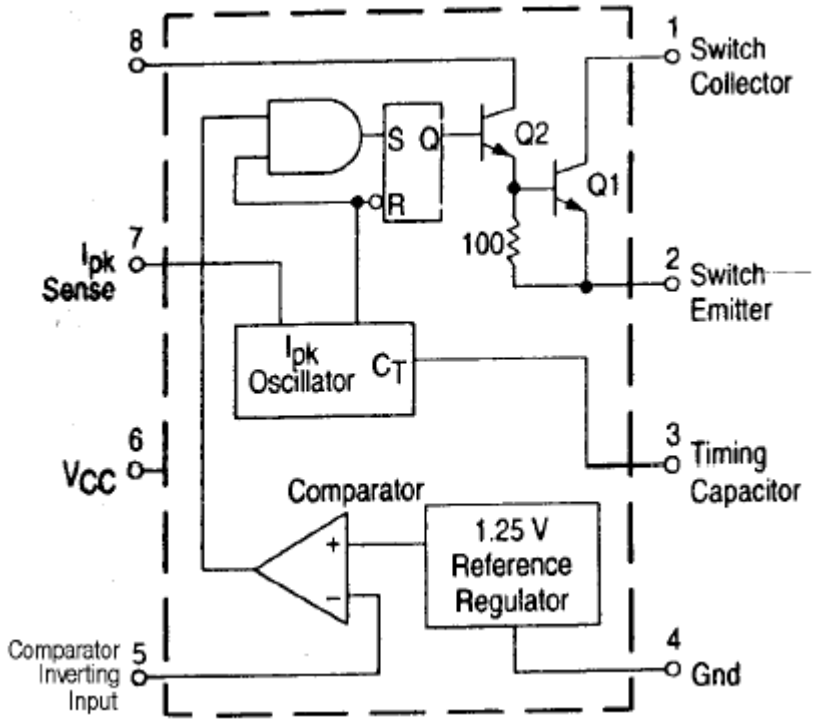
DESCRIPTION

MC34063 is a monolithic control circuit containing the primary functions required for DC-to-DC converters These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

FEATURES

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference
- 8 pin DIP and SO package

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (for IC in Package)

Rating	Symbol	Value	Unit
Power Supply Voltage	Vcc	40	Vdc
Comparator Input Voltage Range	VIR	-0.3 to +40	Vdc
Switch Collector Voltage	VC(switch)	40	Vdc
Switch Emitter Voltage (V_{PIN1} = 40 V)	VE(switch)	40	Vdc
Switch Collector to Emitter Voltage	VCE(switch)	40	Vdc
Driver Collector Voltage	VC(driver)	40	Vdc
Driver Collector Current (Note 1)	IC(driver)	100	mA
Switch Current	I_{SW}	1.5	A
Storage Temperature Range	Tstg	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Vcc = 5.0 V, TA = T_{low} to T_{high} unless otherwise specified, for IC in Package)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{pin5} = 0V, C_T = 1.0 nF, T_A = 25°C)	f_{OSC}	24	33	42	kHz
Charge Current (VCC = 5.0V to 40V, TA = 25°C)	I_{chg}	24	35	42	μA
Discharge Current (V_{CC} = 5.0V to 40V, T_A = 25°C)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25°C)	I_{dischg}/ I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	Vipk(sence)	250	300	350	mV
OUTPUT SWITCH					
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage, Darlington Connection (ISW = 1.0 A, R_{pin} 8 = 82Ω to V_{CC} , Forced β ≅ 20)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, VCE = 5.0 V, TA = 25□C)	h_{FE}	50	75	–	–
Collector Off-State Current (V_{CE} = 40 V)	$I_{C(off)}$	–	40	100	μA
COMPARATOR					
Threshold Voltage (T_A=25°C) (T_A =T_{low} to T_{high})	Vth	1.225 1.21	1.25 –	1.275 1.29	V
Threshold Voltage Line Regulation (Vcc=3.0 V to 40 V)	Reg_{line}	–	1.4	5.0	mV
Input Bias Current (Vin=0 V)	I_{IB}	—	-20	-400	nA
TOTAL DEVICE					
Supply Current (Vcc = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, Vpin 5 > Vth, Pin 2 = Gnd, remaining pins open)	I_{CC}	–	–	4.0	mA

Figure 1. Step-Up Converter

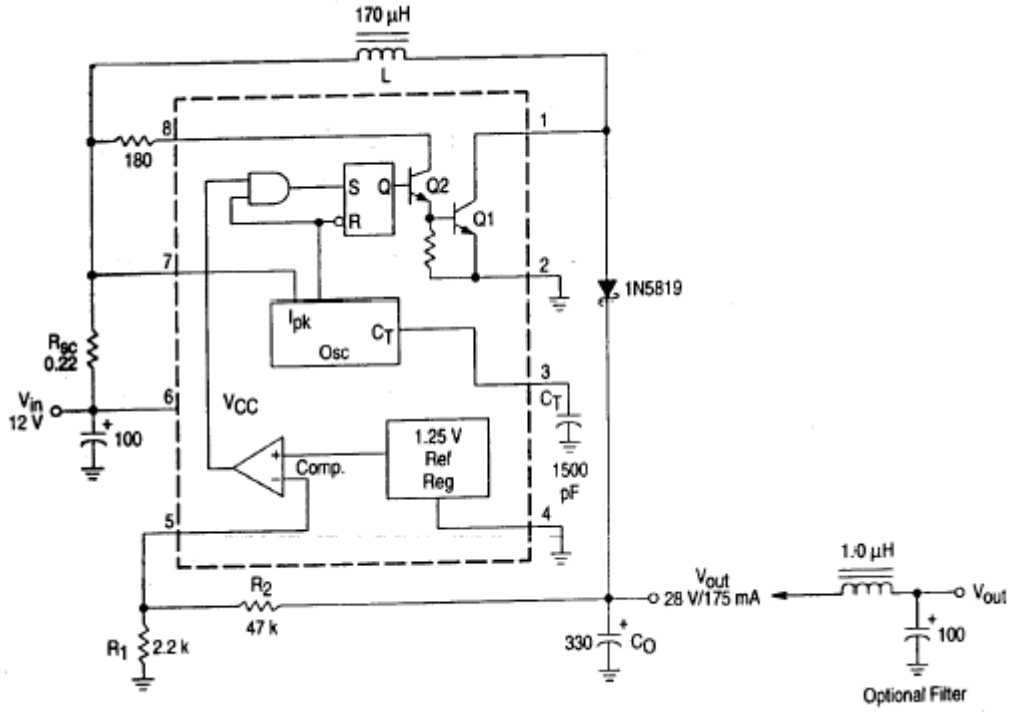
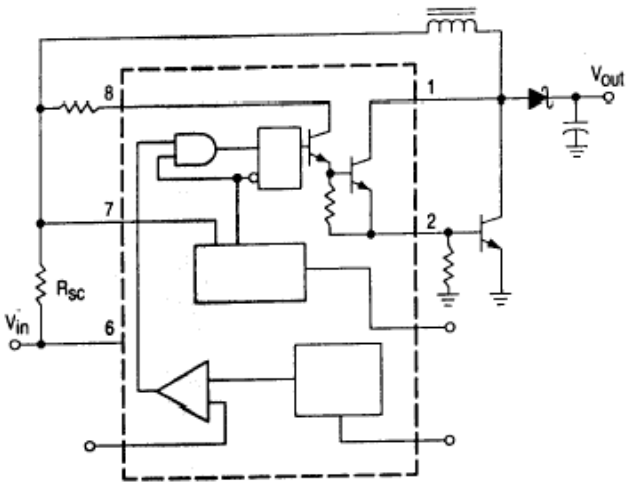


Figure 2. External Current Boost Connections for IC Peak Greater than 1.5 A

2.a External NPN Switch



2.b External NPN Saturated Switch

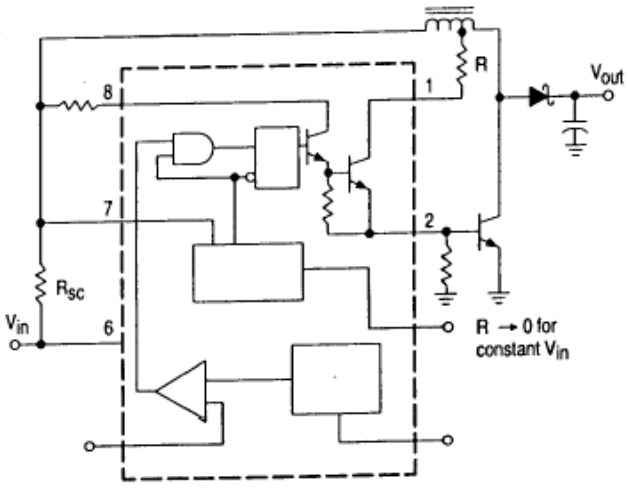


Figure 3. Step-Down Converter

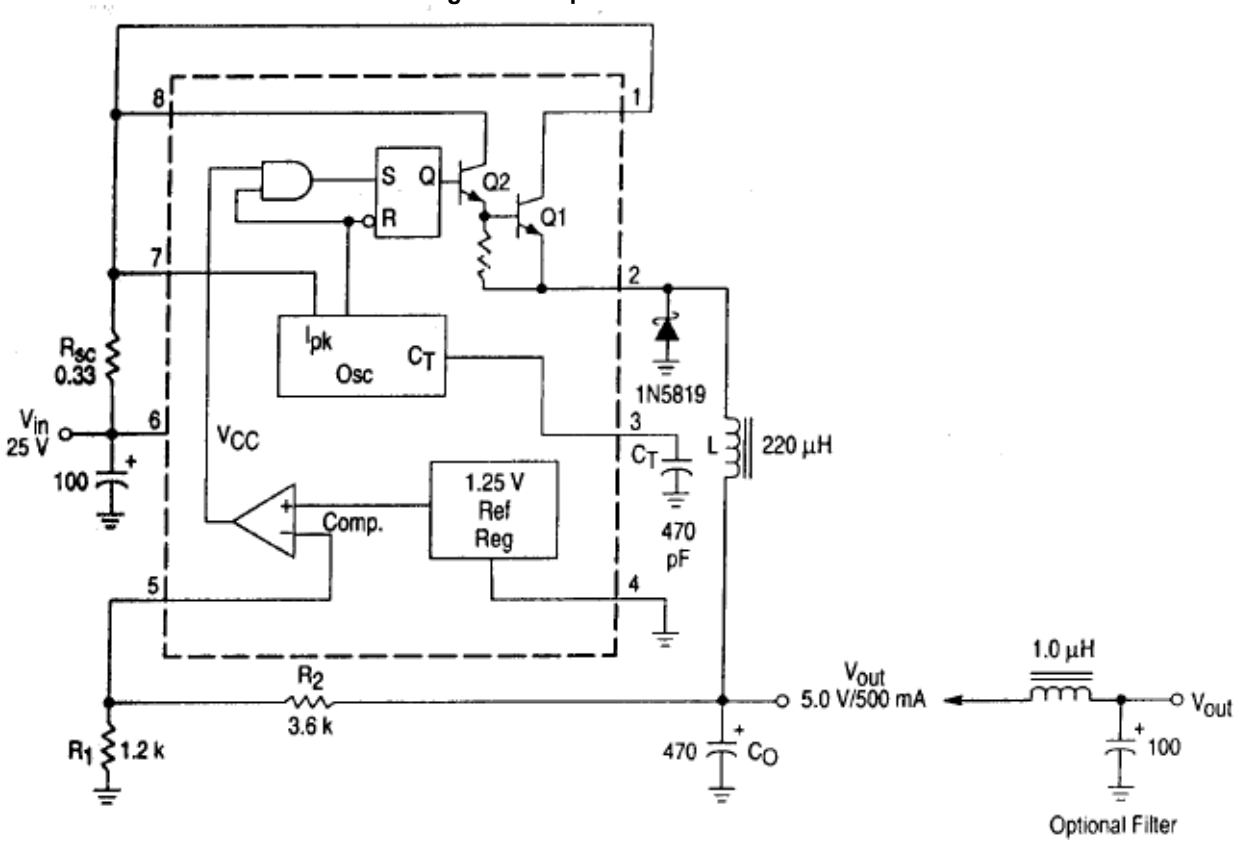
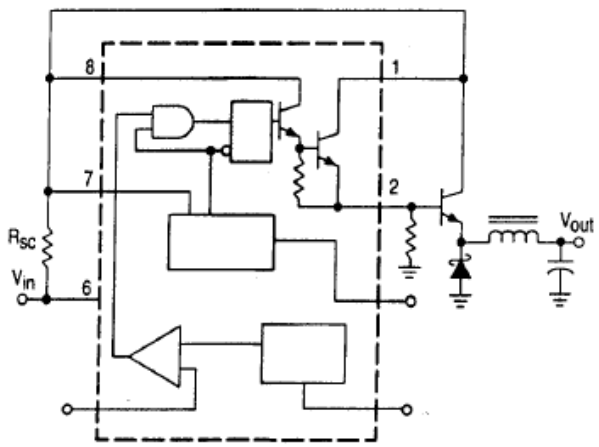


Figure 4. External Current Boost Connections for IC Peak Greater than 1.5 A

4.a External NPN Switch



4.b External NPN Switch

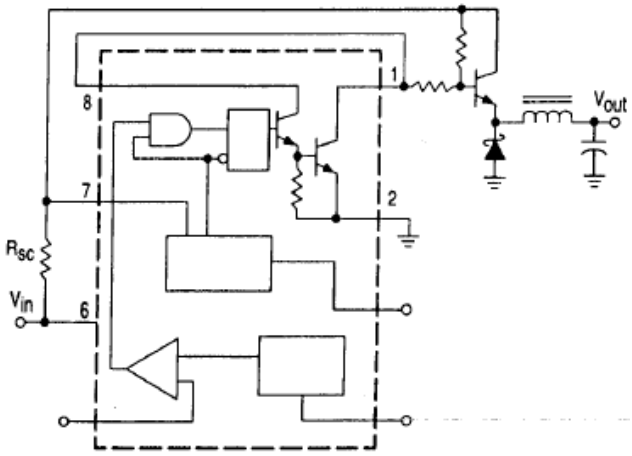


Figure 5. Voltage Inverting Converter

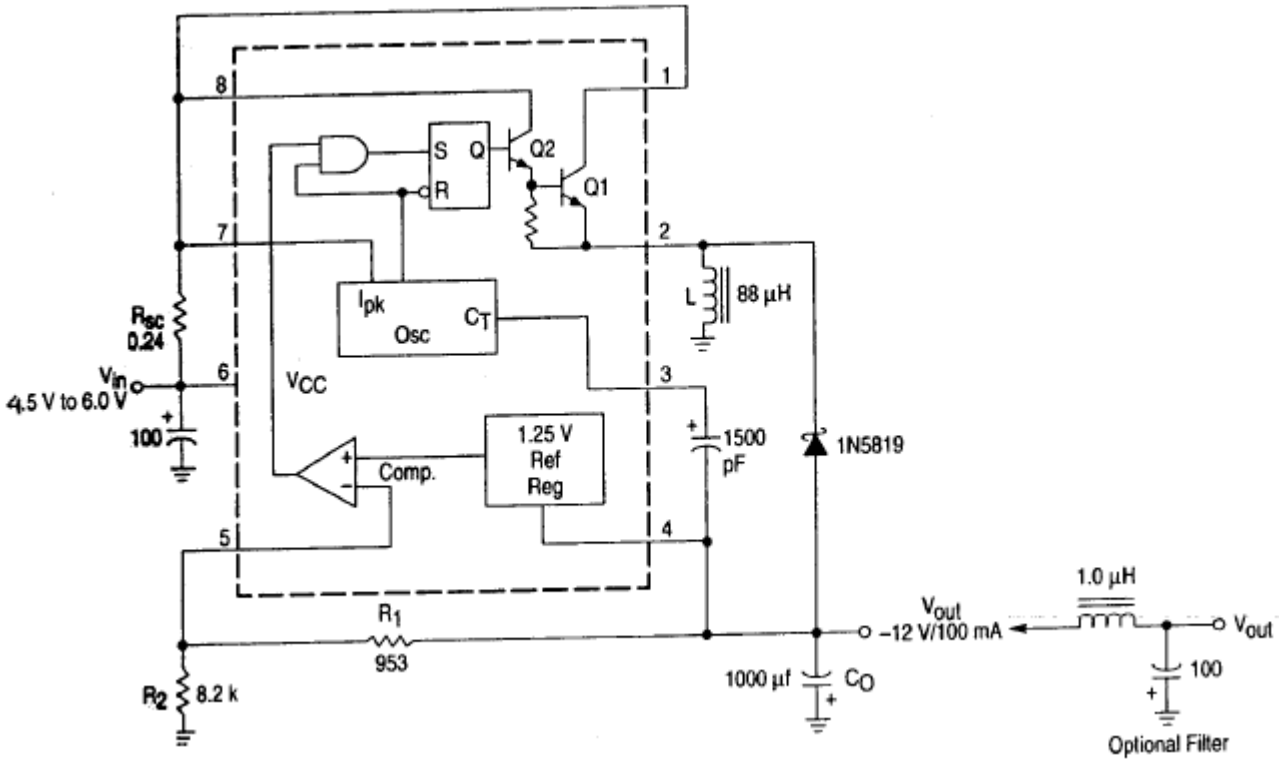
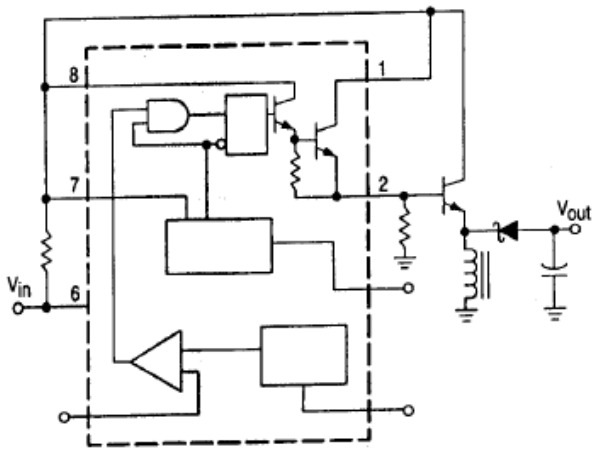


Figure 6. External Current Boost Connections for IC Peak Greater than 1.5 A

6.a External NPN Switch



6.b External NPN Saturated Switch

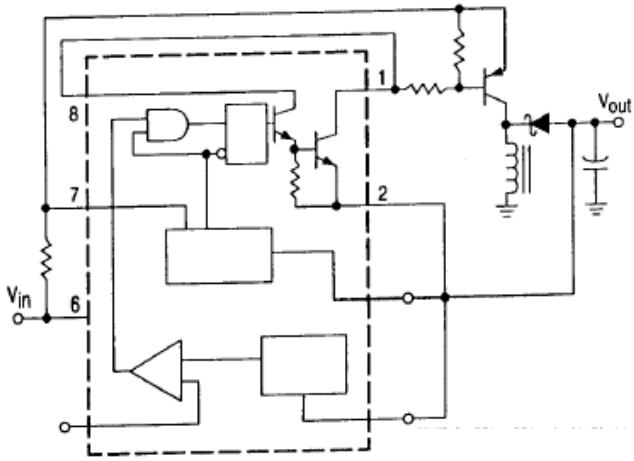


Figure 7. Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in(min)} + V_{sat}}$
$(t_{on}+t_{off})max$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left[\frac{t_{on}}{t_{off}} + 1\right]$	$2I_{out(max)}$	$2I_{out(max)}\left[\frac{t_{on}}{t_{off}} + 1\right]$
R_{SC}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left[\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right] = t_{on(max)}$	$\left[\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right] = t_{on(max)}$	$\left[\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right] = t_{on(max)}$
C_O	$9\frac{I_{out}\ t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\frac{I_{out}\ t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.

V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} - Nominal input voltage.

V_{out} - Desired output voltage,

$$|V_{out}| = 1.25\left[1 + \frac{R_2}{R_1}\right]$$

I_{out} - Desired output current.

f_{min} - Minimum desired output switching frequency at the selected values of Vin and IO.

$V_{ripple(p-p)}$ – Desired peack-to-peack output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.