Dual 900mA Synchronous Buck DC/DC Converter

Features

- Up to 95% Efficiency
- Current mode operation for excellent line and load transient response
- Low quiescent current: 460μA
- Low Switch on Resistance $R_{DS(ON)}$, Internal Switch: 0.35Ω
- Output voltage：0.6V～5.5V
- Automatic PWM/PFM mode switching
- No Schottky diode required
- 1.4MHz fixed frequency switching
- Short-Circuit protection
- Shutdown quiescent current: < 1μA
- Low profile DFN3*3-10L package (lead-free packaging is now available)

Application

- Digital cameras and MP3
- Palmtop computers / PDAs
- Cellular phones
- Wireless handsets and DSL modems
- PC cards
- Portable media players

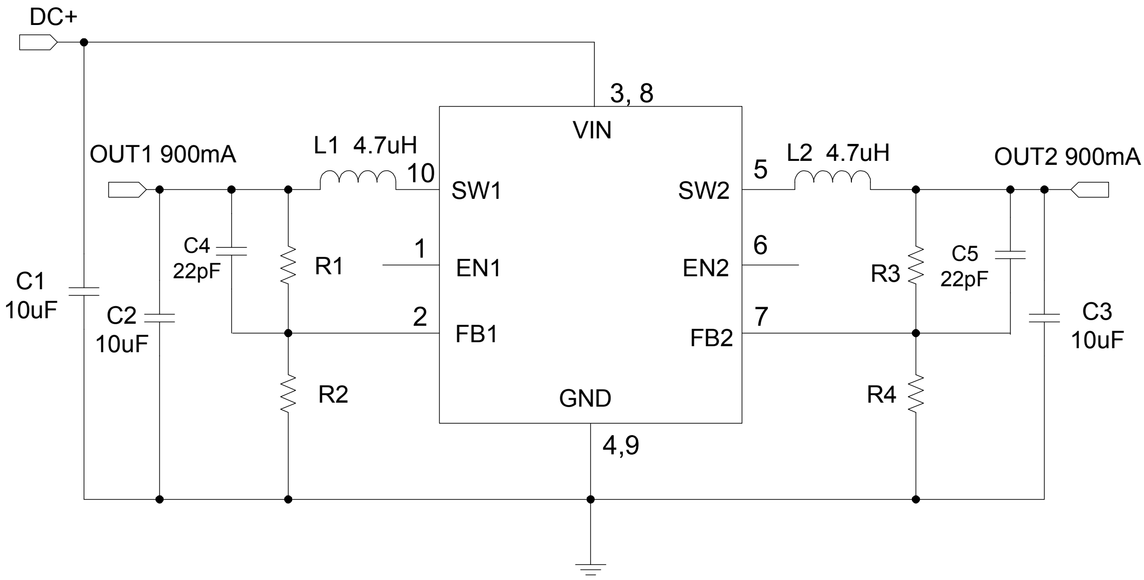
Description

The HM5201 is high efficiency synchronous, dual PWM step-down DC/DC converters working under an input voltage range of 2.5V to 5.5V. This feature makes the HM5201 suitable for single Li-Lon battery-powered applications. 100% duty cycle capability extends battery life in portable devices, while the quiescent current is 200μA with no load, and drops to < 1μA in shutdown.

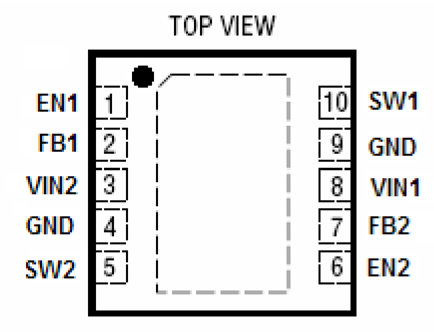
The internal synchronous switch is desired to increase efficiency without an external Schottky diode. The 1.4 MHz fixed switching frequency allows the using of tiny, low profile inductors and ceramic capacitors, which minimized overall solution footprint.

The HM5201 converters are available in the industry standard DFN3*3-10L power packages (or upon request).

Typical Application



Pin Assignment



DFN3*3-10L

PIN NUMBER DFN3*3-10L	PIN NAME	FUNCTION
1	EN1	ON/OFF Control 1 (High Enable)
2	FB1	Output feedback 1
3	VIN2	Input 2
4	GND	Ground
5	SW2	Switch Output 2
6	EN2	ON/OFF Control 2 (High Enable)
7	FB2	Output feedback 2
8	VIN1	Input 1
9	GND	Ground
10	SW1	Switch Output 1

Absolute Maximum Ratings

- Power Dissipation……………………………………………………………………Internally limited
- V_{IN} …………………………………………………………………………………..- 0.3 V ～ + 6 V
- $V_{ON/OFF}$ ……………………………………………..……………………...……- 0.3 V ～ (V_{IN} + 0.3) V
- V_{SW} ……………………………………………………………………………- 0.3 V ～ (V_{IN} + 0.3) V
- V_{FB}……………………………………………………………………………….....- 0.3 V ～ + 6 V
- I_{SW} ………………………………………………………………………………………….1.3A
- Operating Temperature Range ……………………………………………...- 40℃ ～ + 85℃
- Lead Temperature (Soldering 10 sec.) ……………………………………………………..+ 300℃
- Storage Temperature Range ……………………………………………………- 65℃ ～ + 150℃
- Junction Temperature …………………………………………………………………………+ 125℃

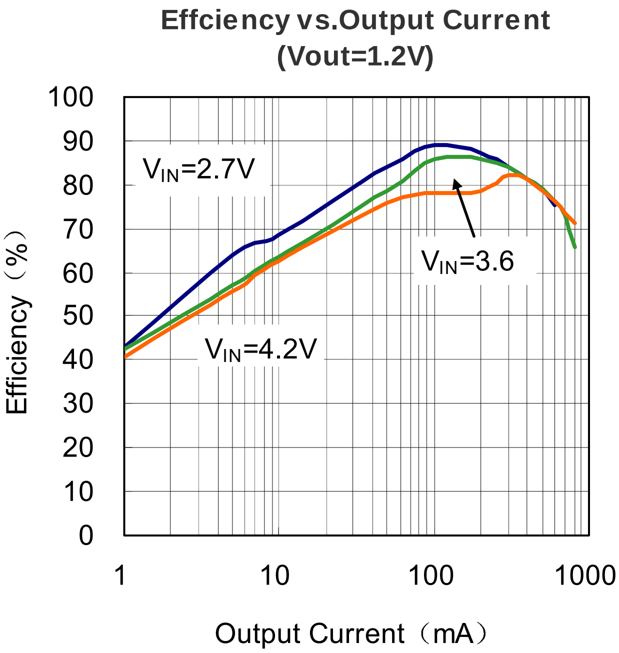
Electrical Characteristics

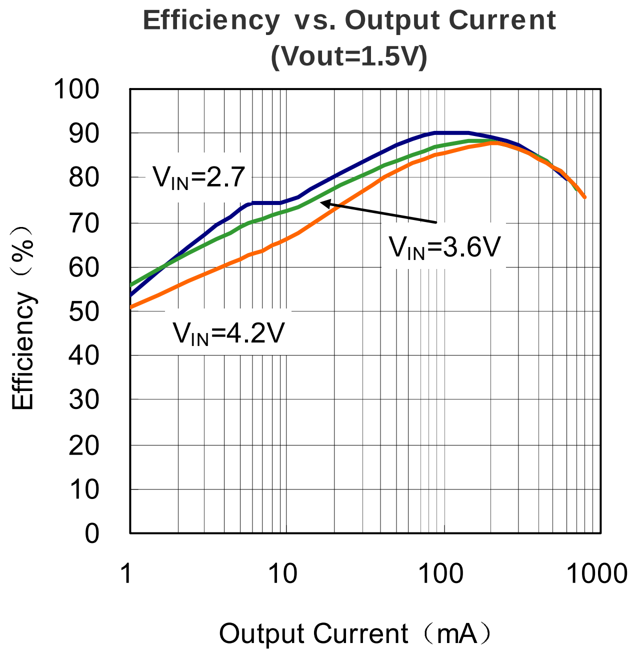
Operating Conditions: T_A=25℃, V_{IN}=3.6V unless otherwise specified.

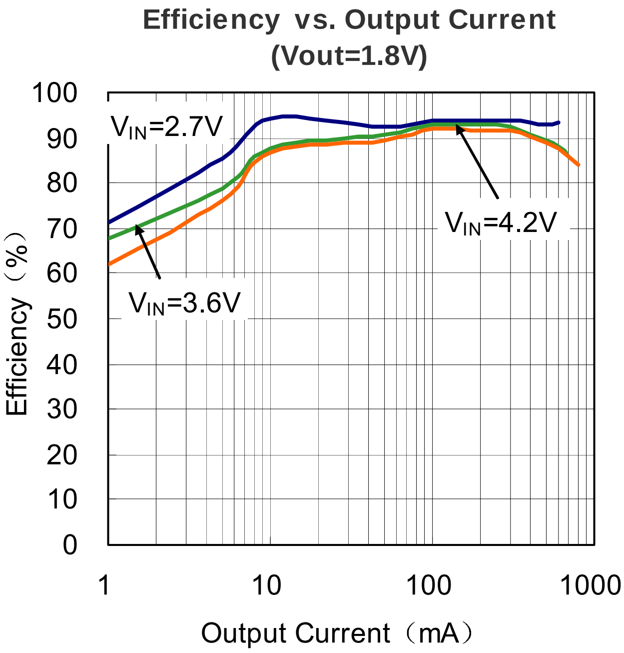
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage	I_{OUT} = 100mA, R2(4)/R1(3)=2	1.75	1.80	1.85	V
V_{IN}	Input Voltage Range		2.5		5.5	V
V_{FB}	Regulated Voltage	T_A = 25℃	0.5880	0.6	0.6120	V
I_{FB}	Feedback Current				±30	nA
ΔV_{FB}	V_{REF}	V_{IN}=2.5V~5.5V		0.03	0.4	%/V
F_{OSC}	Oscillator Frequency	V_{FB} = 0.6V or V_{OUT} = 100%	1.1	1.4	1.7	MHz
I_Q	Quiescent Current	V_{FB} = 0.5V or V_{OUT} = 90%, I_{LOAD} = 0A		200	300	μA
I_S	Shutdown Current	V_{EN} = 0V, V_{IN} = 4.2V		0.1	1	μA
I_{PK}	Peak Inductor Current	V_{IN} = 3V, V_{FB} = 0.5V or V_{OUT} = 90%, Duty Cycle < 35%	0.75	0.9	1	A
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA		0.3		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = -100mA		0.39		Ω
EFFI *	Efficiency	When connected to ext. components V_{IN}=EN=3.6 V, I_{OUT}=100mA		93		%
ΔV_{OUT}	V_{OUT} Line Regulation	V_{IN}=2.5V~5.5V		0.03	0.3	%/V
$V_{LOADREG}$	V_{OUT} Load Regulation			0.33		%

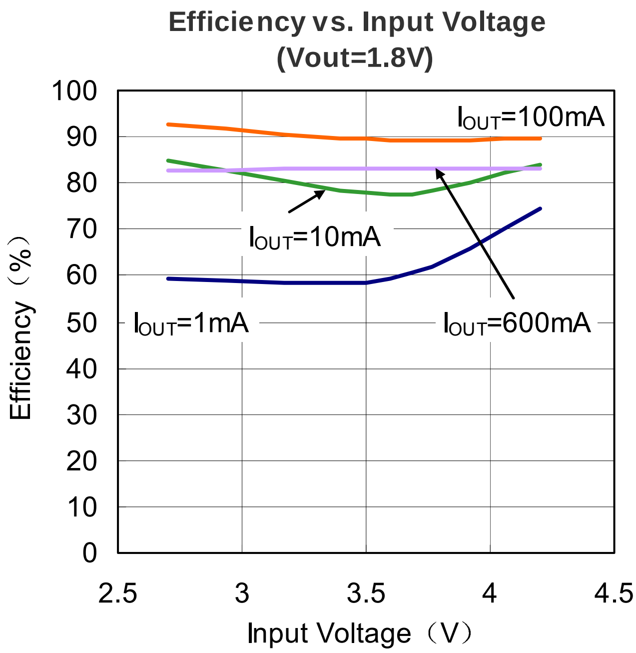
⋆ EFFI = [(Output Voltage × Output Current) / (Input Voltage × Input Current)] × 100%

Typical Performance Characteristics

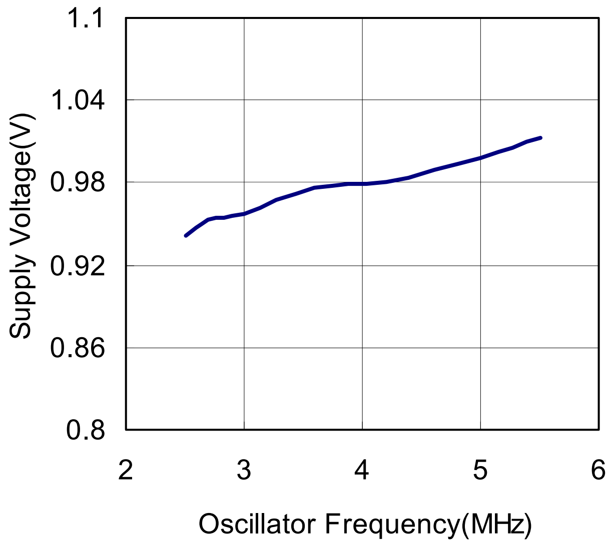




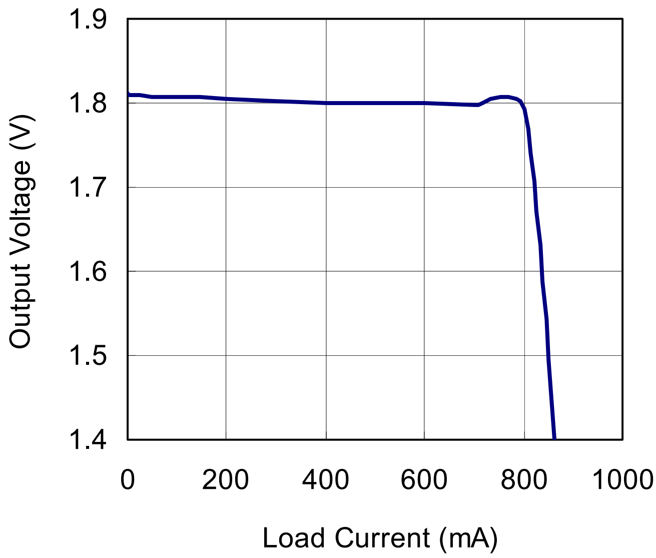




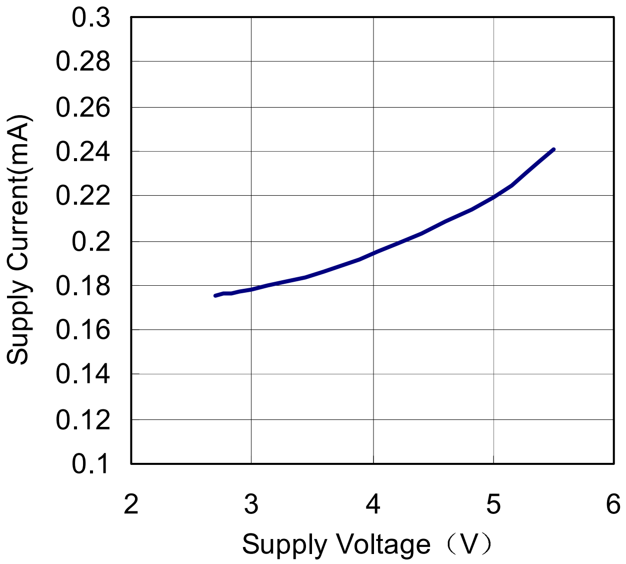
Oscillator Frequency vs. Supply Voltage(Vout=1.8V Io=100mA)



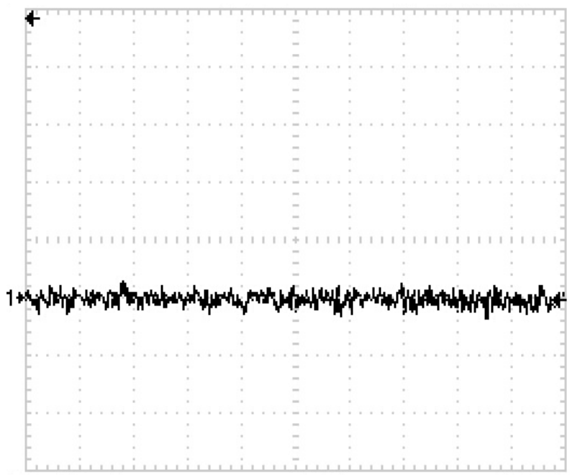
Output Voltage vs. Load Current(Vin=3.6V)



Supply Current vs Supply Voltage (Vout=1.8V Io=0A)

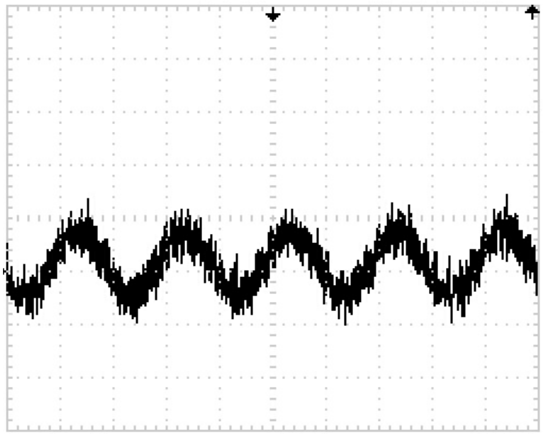


Output Noise（100mV/DIV 2ms/DIV AC COUPLED）



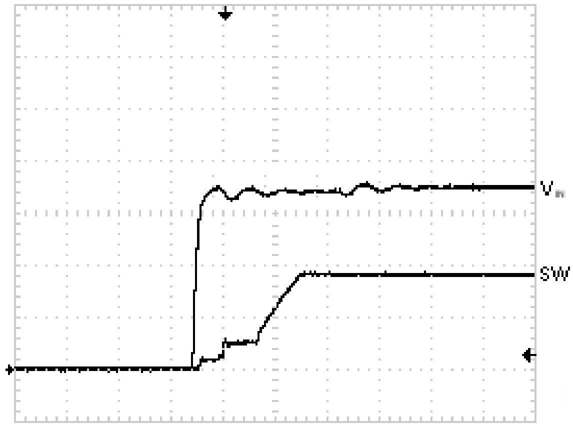
V_{IN}=3.6V V_{OUT}=1.8V I_{LOAD}=0mA

Output Noise（20mV/DIV 10ms/DIV AC COUPLED）



V_{IN}=3.6V V_{OUT}=1.8V I_{LOAD}=200mA

Start –up from Shutdown Input and Output Noise（1V/DIV 100ns/DIV）



Application Information

PIN ASSIGNMENT

EN1 (Pin 1): First en control Input. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave EN floating.

FB1(Pin 2): Output feedback 1. Receive the feedback voltage from an external resistive divider across the output. In the adjustable version, the output voltage is set by a resistive divider according to the following formula: $V_{OUT1} = 0.6V \cdot [1 + (R1/R2)]$.

VIN2 (Pin 3): Second main Supply Pin. It must be closely decoupled to GND, or with a 10μF or greater ceramic capacitor.

GND (Pin 4，9): Ground Pin.

SW2 (Pin 5): Second switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

EN2 (Pin 6): Second en control Input. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave EN floating.

FB2(Pin 7): Output feedback 2. Receive the feedback voltage from an external resistive divider across the output. In the adjustable version, the output voltage is set by a resistive divider according to the following formula: $V_{OUT2} = 0.6V \cdot [1 + (R3/R4)]$.

VIN1 (Pin 8): First main Supply Pin .It must be closely decoupled to GND, or with a 10μF or greater ceramic capacitor.

SW1 (Pin 10): First switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

Application Information

The basic HM5201 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by CIN and COUT.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 4.7µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation 1. A reasonable starting point for setting ripple current is $\triangle I_L$ = 360mA (40% of 900mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 1.08A rated inductor should be enough for most applications (900mA + 180mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the HM5201 requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at V_{IN} = $2V_{OUT}$, where I_{RMS} = $I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).

Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Suggested Inductors

Component Supplier	Series	Inductance (uH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR 3015	2.2	60	1480	3 x 3 x 1.5
TAIYO YUDEN	NR 3015	4.7	120	1020	3 x 3 x 1.5
Sumida	CDRH2D14	2.2	75	1500	4.5 x 3.2 x 1.55
Sumida	CDRH2D14	4.7	135	1000	4.5 x 3.2 x 1.55
GOTREND	GTSD32	2.2	58	1500	3.85 x 3.85 x 1.8
GOTREND	GTSD32	4.7	146	1100	3.85 x 3.85 x 1.8

Suggested Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (uF)	Case Size
TDK	C1608JB0J475M	4.7	0603
TDK	C2012JB0J106M	10	0805
MURATA	GRM188R60J475KE19	4.7	0603
MURATA	GRM219R60J106ME19	10	0805
MURATA	GRM219R60J106KE19	10	0805
TAIYO YUDEN	JMK107BJ475RA	4.7	0603
TAIYO YUDEN	JMK107BJ106MA	10	0603
TAIYO YUDEN	JMK212BJ106RD	10	0805

Efficiency Considerations

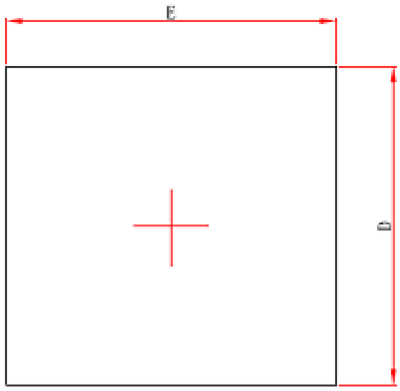
The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and I^2R losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge △Q moves from VIN to ground. The resulting △Q/△t is the current out of VIN that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f (Q_T+Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

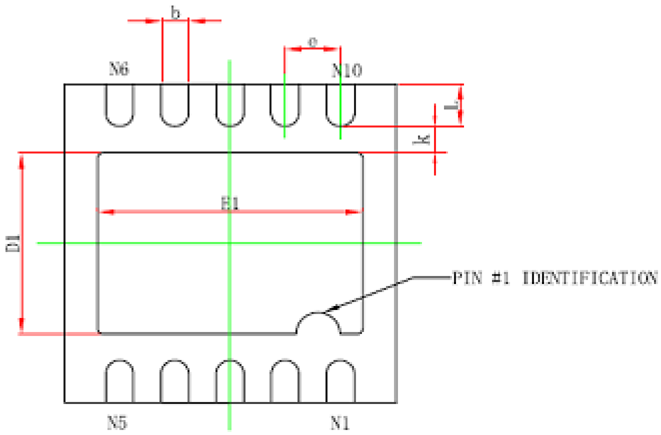
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1\text{-}DC)$ The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Packaging Information

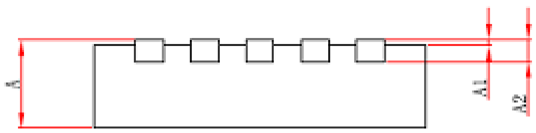
DFN3*3-10L Package Outline Dimension



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A2	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	2.300	2.500	0.091	0.098
k	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020