

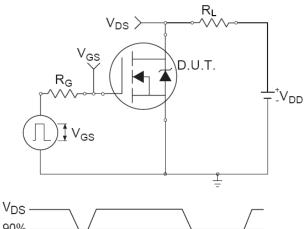
## Features

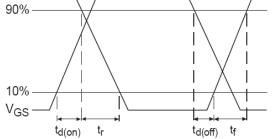
- $V_{DSS}=40V/V_{GSS}=\pm 20V/I_D=130A$  $R_{DS(ON)}=4m\Omega(max.)@V_{GS}=10V$
- High Dense Cell Design
- Reliable and Rugged
- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance

# **Applications**

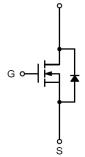
- Power Management in Inverter System
- Synchronous Rectification "

# Switching Time Test Circuit and Waveforms





# **Pin Description**





#### Marking and pin Assignment



TO-220-3L top view

#### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM1404B	HM1404B	TO-220-3L	-	-	-



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# **Absolute Maximum Ratings** (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Typical	Unit
V <sub>DSS</sub>	Drain-Source Voltage	40	V
V <sub>GSS</sub>	Gate –Source Voltage	±20	V
т	Continuous Drain Current	C 100	Α
I <sub>D</sub>	Continuous Drain Current	130	Α
I <sub>DP</sub>	300us Pulsed Drain Current Tested $T_{C}=25^{\circ}C$	300	Α
Is	Diode Continuous Forward Current	30	Α
T <sub>J</sub>	Operating Junction Temperature	150	°C
T <sub>STG</sub>	Storage Temperature Range	-55 ~ 150	°C

## **Electrical Characteristics** (TA=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур	Max.	Unit
Static Char	racteristics					
<b>BV</b> <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V,I <sub>D</sub> =250uA	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS}=32V, V_{GS}=0V$			100	uA
V <sub>GS(th)</sub>	Gate Threshold Voltage	$T_{J}=85^{\circ}C$ $V_{DS}=V_{GS},I_{D}=250uA$	1	2	$\frac{1}{3}$	V
I <sub>GSS</sub>	Gate Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	_	±100	nA
$R_{DS(on)}^{1}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=30A$		3.2	4	mΩ
	racteristics					
$V_{SD}^{1}$	Diode Forward Voltage	$I_{SD}=30A, V_{GS}=0V$		0.85	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	$I_{SD}=30A$ ,		50		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>SD</sub> /dt=100A/us		90		nC
Dynamic C	<sup>2</sup> haracteristics <sup>2</sup>				-	
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, Frequency=1MHz		1.5		Ω
C <sub>iss</sub>	Input Capacitance	1 2		4500		pF
C <sub>oss</sub>	Output Capacitance	$V_{GS}=0V, V_{DS}=20V$		800		
C <sub>rss</sub>	Reverse Transfer Capacitance	Frequency=1MHz		240		
t <sub>d(on)</sub>	Turn-On Delay Time	V -20V D -200		19		
t <sub>r</sub>	Turn-On Rise Time	$V_{DD}=20V, R_{L}=30\Omega$		14		ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$I_D=1.0A, V_{GEN}=10V$ $R_G=6\Omega$		60		
$t_{f}$	Turn-Off Fall Time	NG-022		35		
Gate Charg	ge Characteristics <sup>2</sup>					
Qg	Total Gate Charge	V = 20V V = 10V		85		nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{DS}=20V, V_{GS}=10V$		30		
Q <sub>gd</sub>	Gate-Drain Charge	I <sub>D</sub> =30A		23		

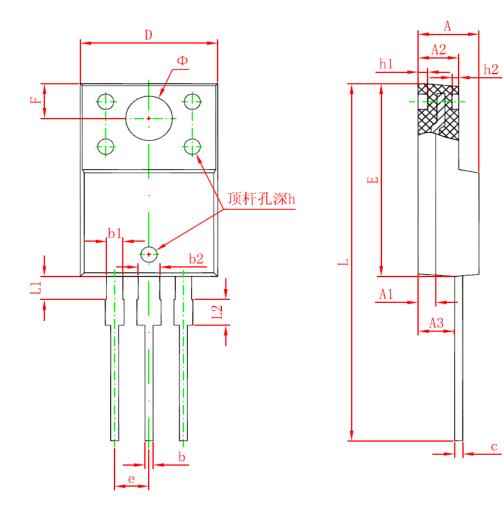
1: Pulse test ; pulse width  $\leq$  300ns, duty cycle  $\leq$  2%.

2: Guaranteed by design, not subject to production testing.

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## **TO-220F PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
A	4.300	4.700	0.169	0.185	
A1	1.300	REF.	0.051 REF.		
A2	2.800	3.200	0.110	0.126	
A3	2.500	2.900	0.098	0.114	
b	0.500	0.750	0.020	0.030	
b1	1.100	1.350	0.043	0.053	
b2	1.500	1.750	0.059	0.069	
С	0.500	0.750	0.020	0.030	
D	9.960	10.360	0.392	0.408	
E	14.800	15.200	0.583	0.598	
e	2.540	TYP.	0.100 TYP.		
F	2.700 REF.		0.106 REF.		
Φ	3.500 REF.		0.138 REF.		
h	0.000	0.300	0.000	0.012	
h1	0.800	REF.	0.031 REF.		
h2	0.500	REF.	0.020 REF.		
L	28.000	28.400	1.102	1.118	
L1	1.700	1.900	0.067	0.075	
L2	1.900	2.100	0.075	0.083	

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