

N-Channel Enhancement Mode Power MOSFET

Description

The HM4260 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

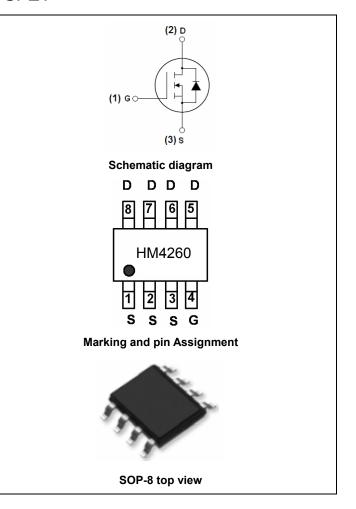
- V_{DS} =60V, I_D =19A $R_{DS(ON)} < 11.5 mΩ @ V_{GS}$ =10V (Typ:9.1mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

100% UIS TESTED!

100% ΔVds TESTED!



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4260	HM4260	SOP-8	-	-	-

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _G S	±20	V
Drain Current-Continuous	I _D	19	Α
Drain Current-Continuous(T _C =100°C)	I _D (100℃)	13.5	А
Pulsed Drain Current	I _{DM}	75	Α
Maximum Power Dissipation	P _D	3	W
Derating factor		0.73	W/℃
Single pulse avalanche energy (Note 5)	E _{AS}	450	mJ
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{ heta JC}$	1.36	°C/W



Electrical Characteristics (T_C=25 ℃ unless otherwise noted)

Parameter Symbol Con		Condition	Min	Тур	Max	Unit
Off Characteristics	<u>.</u>					
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA 60		68	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA 2		3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =15A	-	9.1	11.5	mΩ
Forward Transconductance	g FS	V _{DS} =25V,I _D =15A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{lss}	\/ -25\/\/ -0\/	-	2350	-	PF
Output Capacitance	Coss	V_{DS} =25V, V_{GS} =0V, F=1.0MHz	-	237	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.UIVID2	-	205	-	PF
Switching Characteristics (Note 4)	<u>.</u>					
Turn-on Delay Time	t _{d(on)}		-	16	-	nS
Turn-on Rise Time	t _r	V_{DD} =30V, I_D =2A, R_L =15 Ω	-	10	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_G =2.5 Ω	-	45	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Qg	\/ -20\/ -45A	-	50	-	nC
Gate-Source Charge	Q _{gs}	$V_{DS}=30V,I_{D}=15A,$ $V_{GS}=10V$	-	12	-	nC
Gate-Drain Charge	Q _{gd}	V _{GS} -10V	-	16	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =15A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	19	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF =19A	-	28		nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs(Note3)		49		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

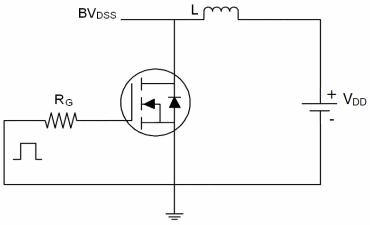
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- **2.** Surface Mounted on FR4 Board, $t \le 10$ sec.
- **3.** Pulse Test: Pulse Width ≤ 300μ s, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- **5.** E_{AS} condition : Tj=25 $^{\circ}$ C,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25 Ω

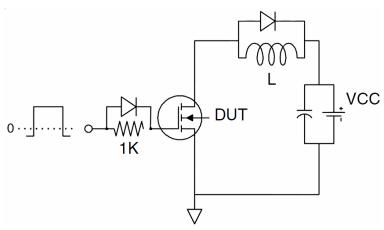


Test Circuit

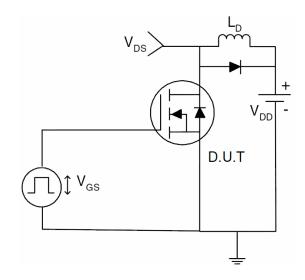
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

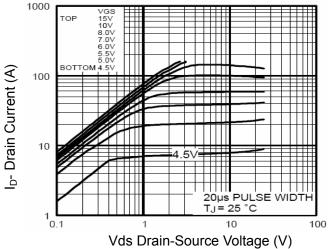


Figure 1 Output Characteristics

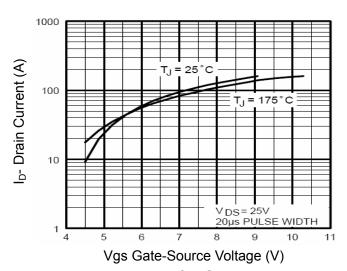


Figure 2 Transfer Characteristics

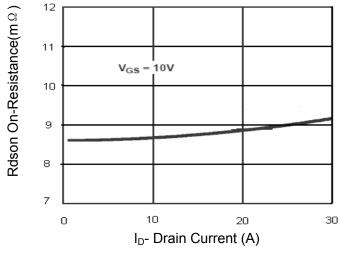


Figure 3 Rdson- Drain Current

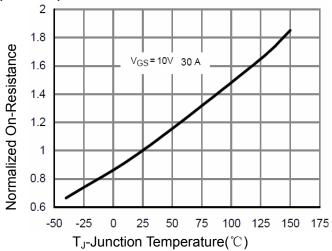


Figure 4 Rdson-JunctionTemperature

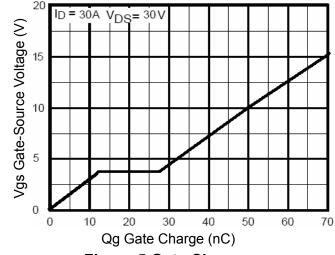


Figure 5 Gate Charge

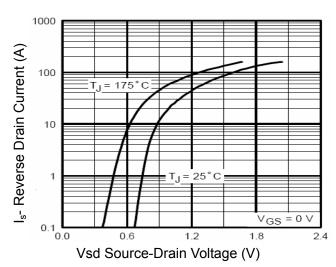


Figure 6 Source- Drain Diode Forward

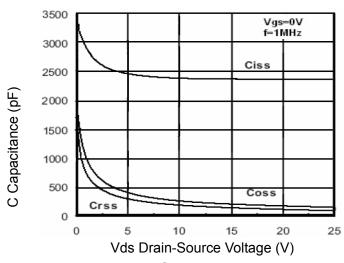


Figure 7 Capacitance vs Vds

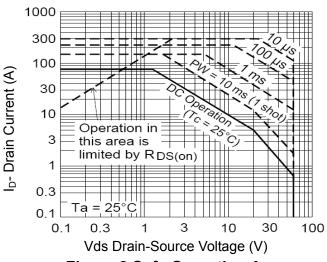


Figure 8 Safe Operation Area

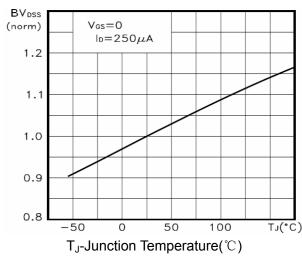


Figure 9 BV_{DSS} vs Junction Temperature

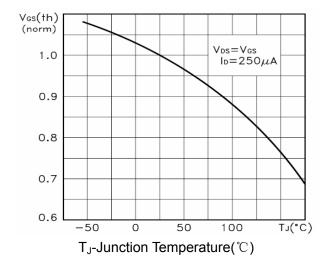


Figure 10 V_{GS(th)} vs Junction Temperature

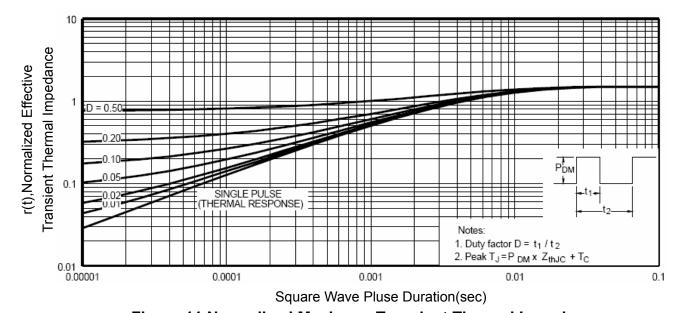
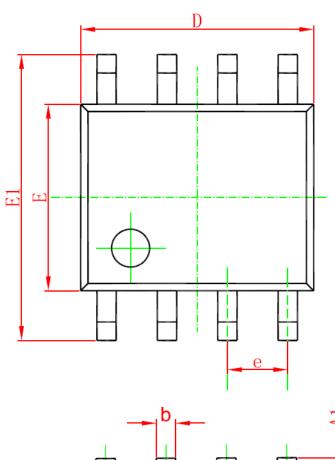
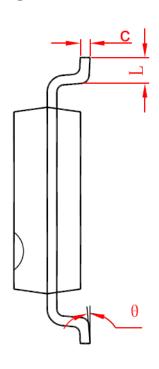


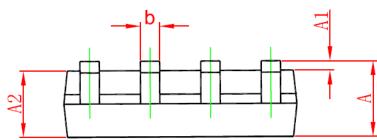
Figure 11 Normalized Maximum Transient Thermal Impedance



SOP-8 PACKAGE IN FORMATION







Symbol	Dimensions In	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	1. 350	1. 750	0. 053	0. 069	
A1	0. 100	0. 250	0.004	0. 010	
A2	1. 350	1. 550	0.053	0. 061	
b	0. 330	0. 510	0. 013	0. 020	
С	0. 170	0. 250	0.006	0. 010	
D	4. 700	5. 100	0. 185	0. 200	
Е	3. 800	4. 000	0. 150	0. 157	
E1	5. 800	6. 200	0. 228	0. 244	
е	1. 270 (BSC)		0. 050 (BSC)		
L	0. 400	1. 270	0. 016	0. 050	
θ	0°	8°	0°	8°	

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