

## Description

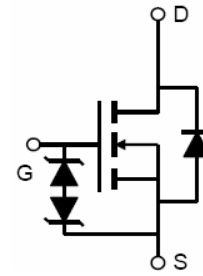
The HM4402E uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

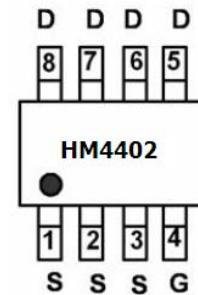
- $V_{DS} = 20V, I_D = 14A$   
 $R_{DS(ON)} < 7\ m\Omega @ V_{GS} = 4.5V$   
 $R_{DS(ON)} < 9\ m\Omega @ V_{GS} = 2.5V$   
 ESD Rating: 2000V HBM
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

## Application

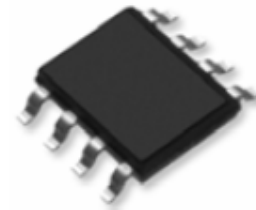
- PWM application
- Load switch



Schematic diagram



Marking and pin Assignment



SOP-8 top view

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4402E	HM4402E	SOP-8	Ø330mm	12mm	2500 units

## Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current-Continuous	$I_D$	14	A
Pulsed Drain Current	$I_{DM}$	44	A
Maximum Power Dissipation	$P_D$	3	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	42	$^\circ C/W$
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## Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

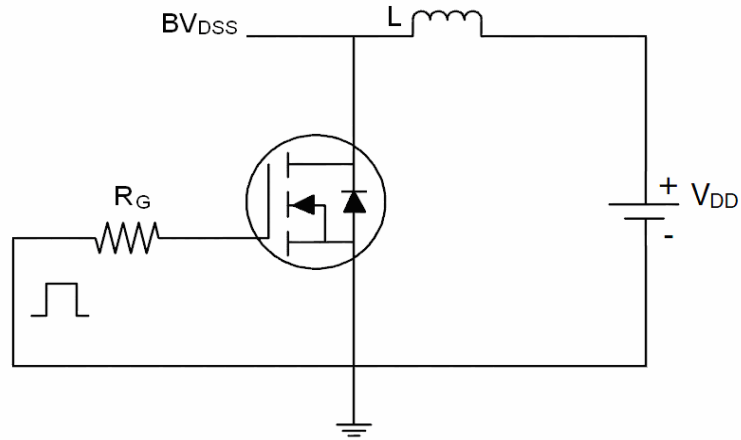
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	20	22	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	-	±10	μA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.6	0.8	1.2	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	5	7	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5.5A	-	7	9	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =10A	30	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, F=1.0MHz	-	1710	-	PF
Output Capacitance	C <sub>oss</sub>		-	232	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	200	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, R <sub>L</sub> =1Ω V <sub>GS</sub> =10V, R <sub>GEN</sub> =3Ω	-	2.5	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	7.2	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	49	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	10.8	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =10A, V <sub>GS</sub> =4.5V	-	17.5	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	4.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	14	A

### Notes:

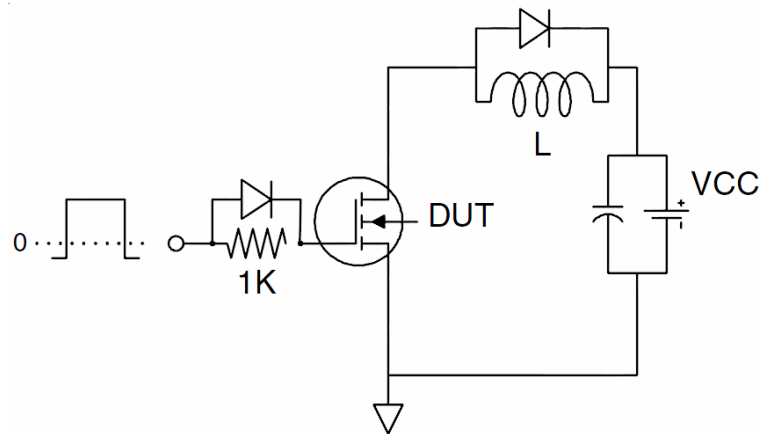
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

**Test Circuit**

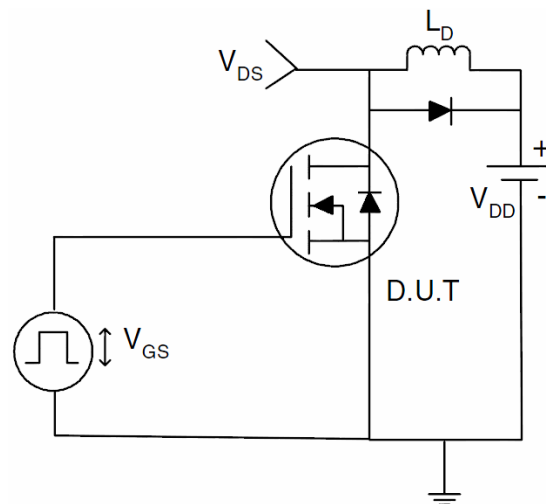
**1) E<sub>AS</sub> test Circuits**



**2) Gate charge test Circuit**



**3) Switch Time Test Circuit**



Typical Electrical and Thermal Characteristics

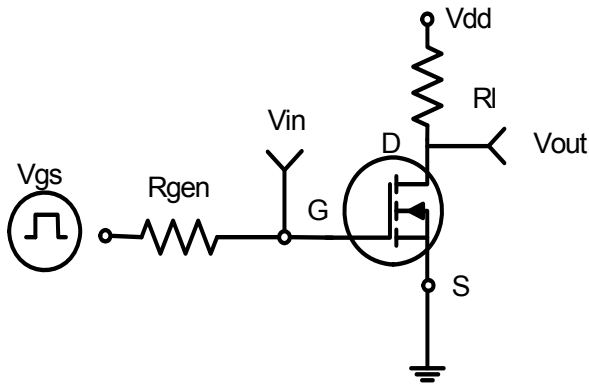


Figure 1: Switching Test Circuit

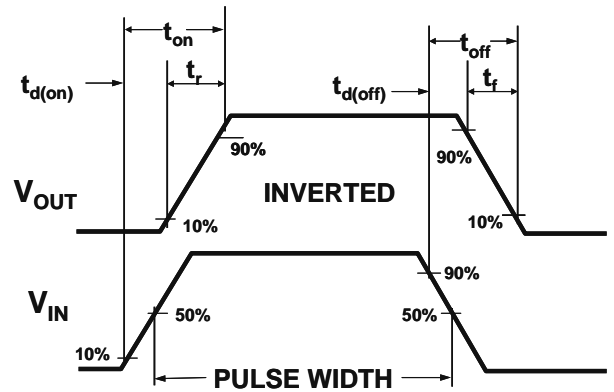


Figure 2: Switching Waveforms

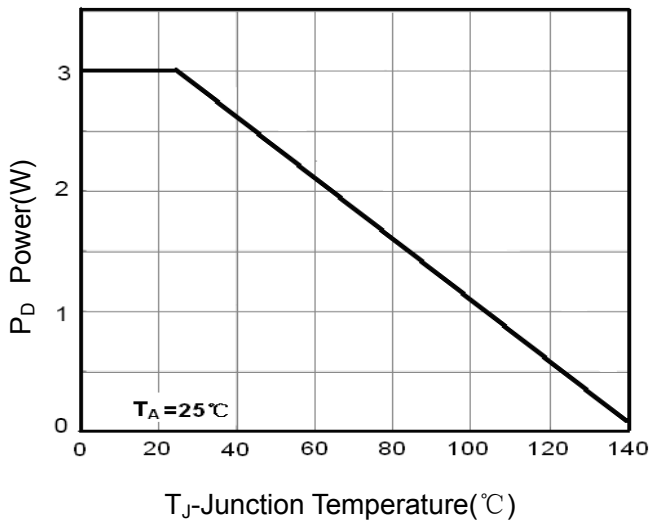


Figure 3 Power Dissipation

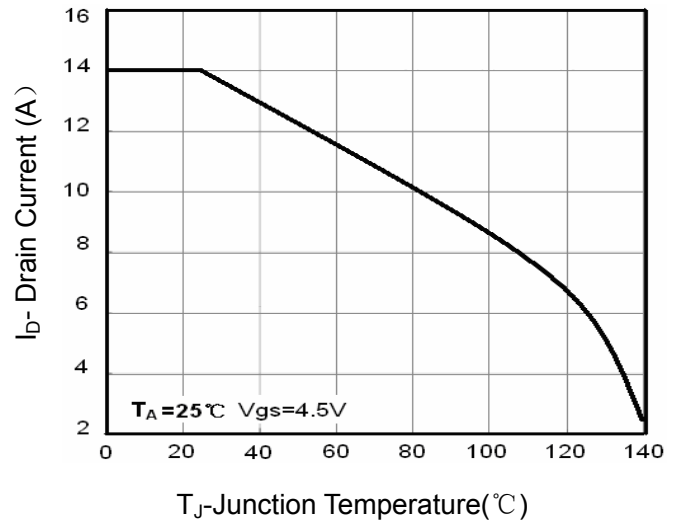


Figure 4 Drain Current

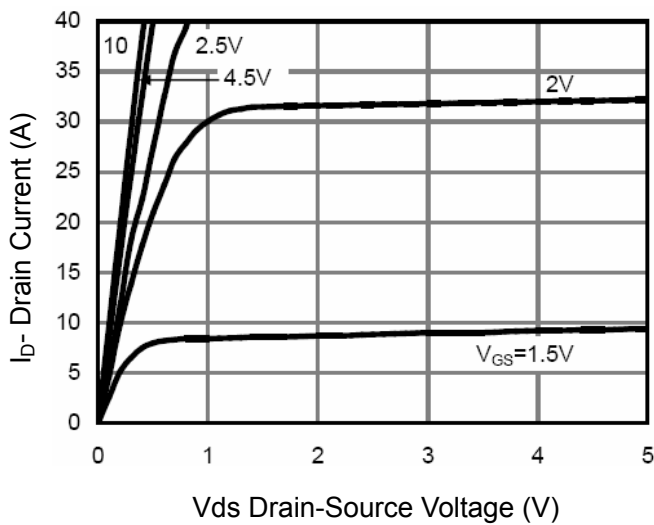


Figure 5 Output Characteristics

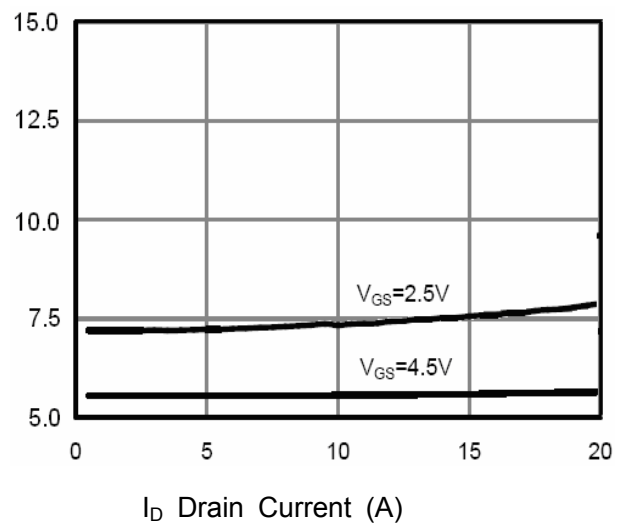
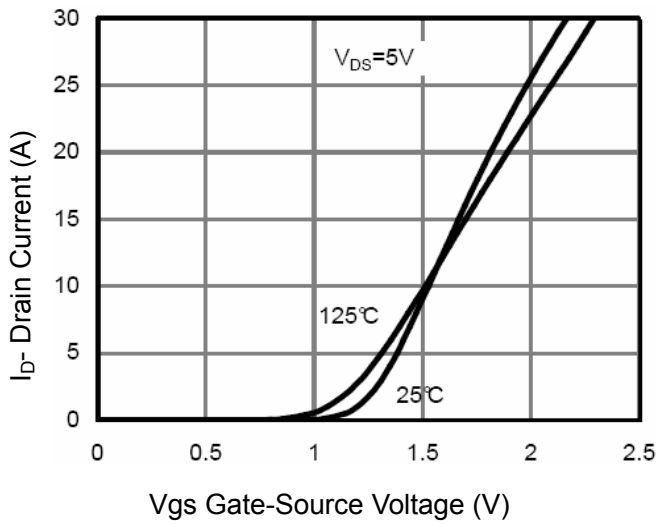
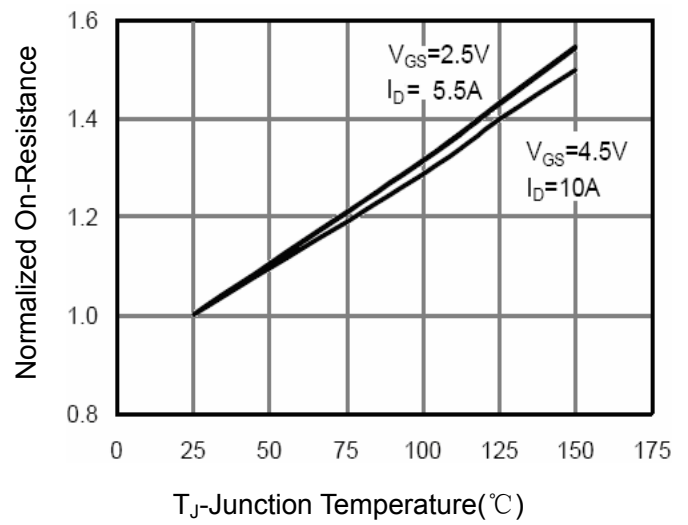


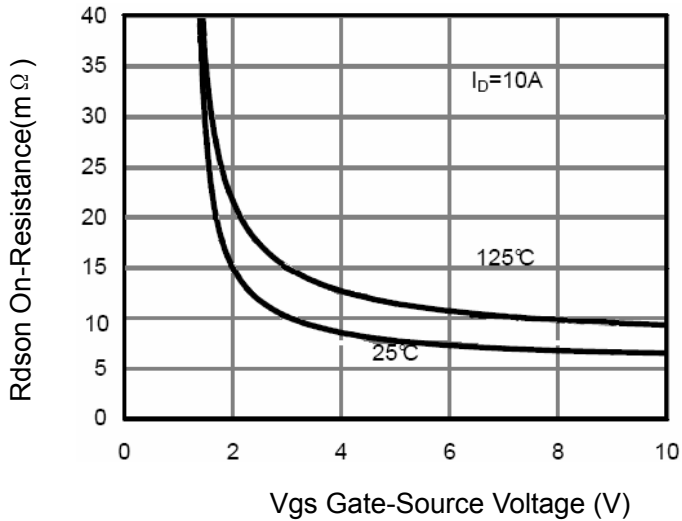
Figure 6 Drain-Source On-Resistance



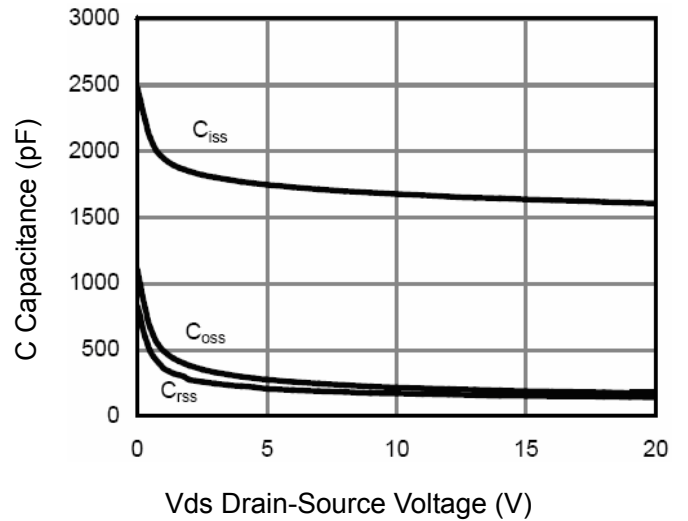
**Figure 7 Transfer Characteristics**



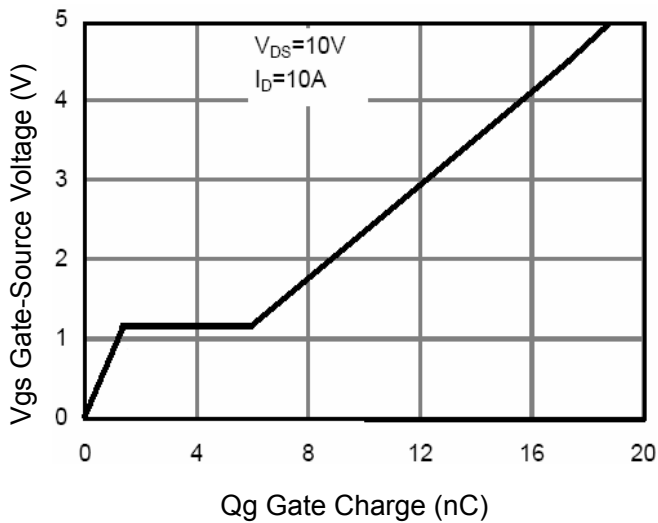
**Figure 8 Drain-Source On-Resistance**



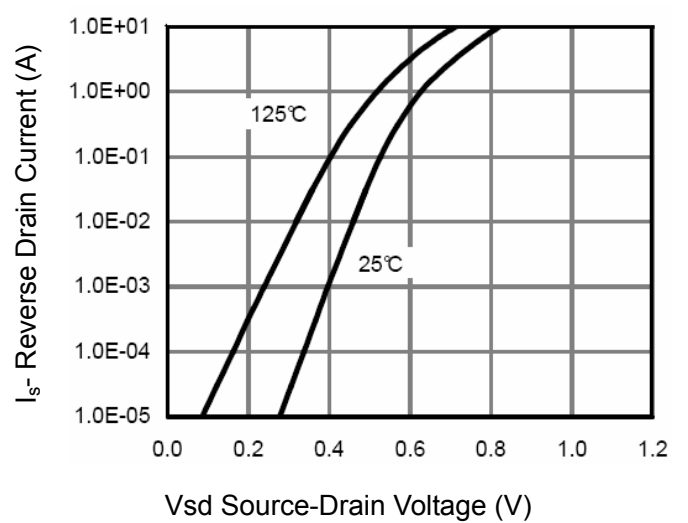
**Figure 9 Rdson vs Vgs**



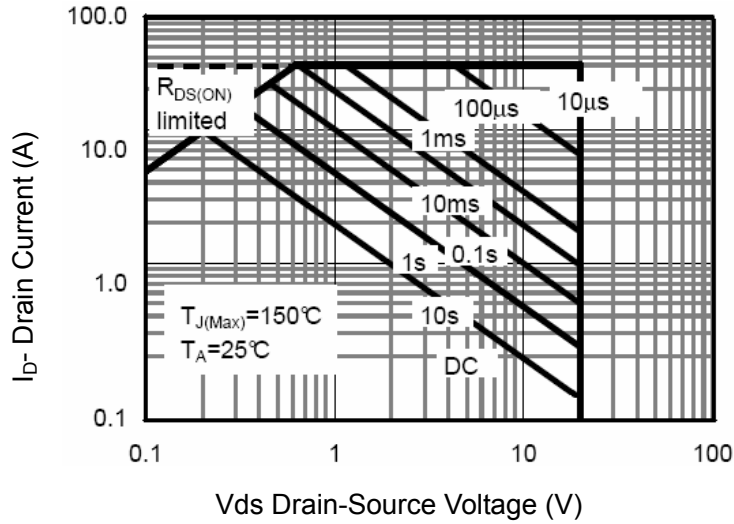
**Figure 10 Capacitance vs Vds**



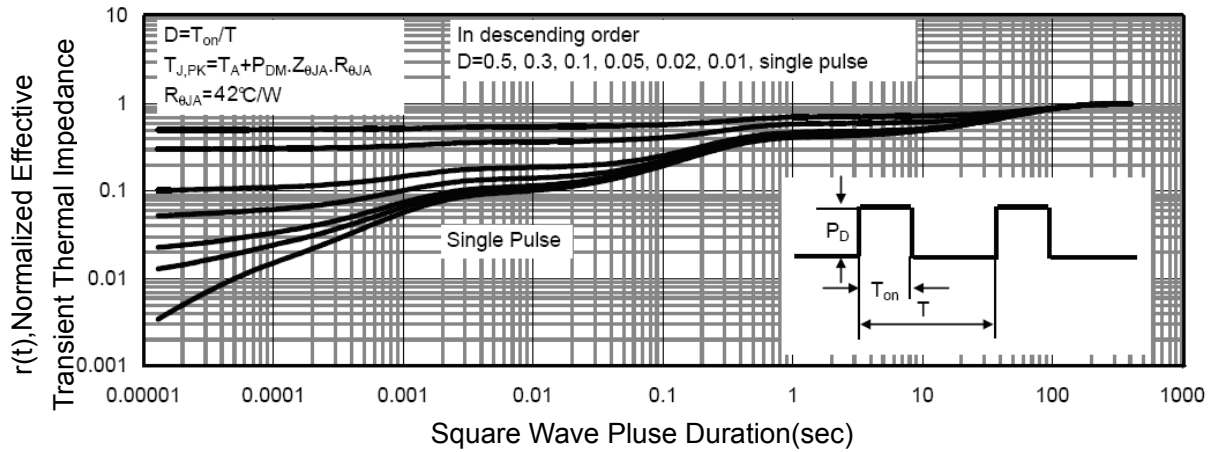
**Figure 11 Gate Charge**



**Figure 12 Source- Drain Diode Forward**

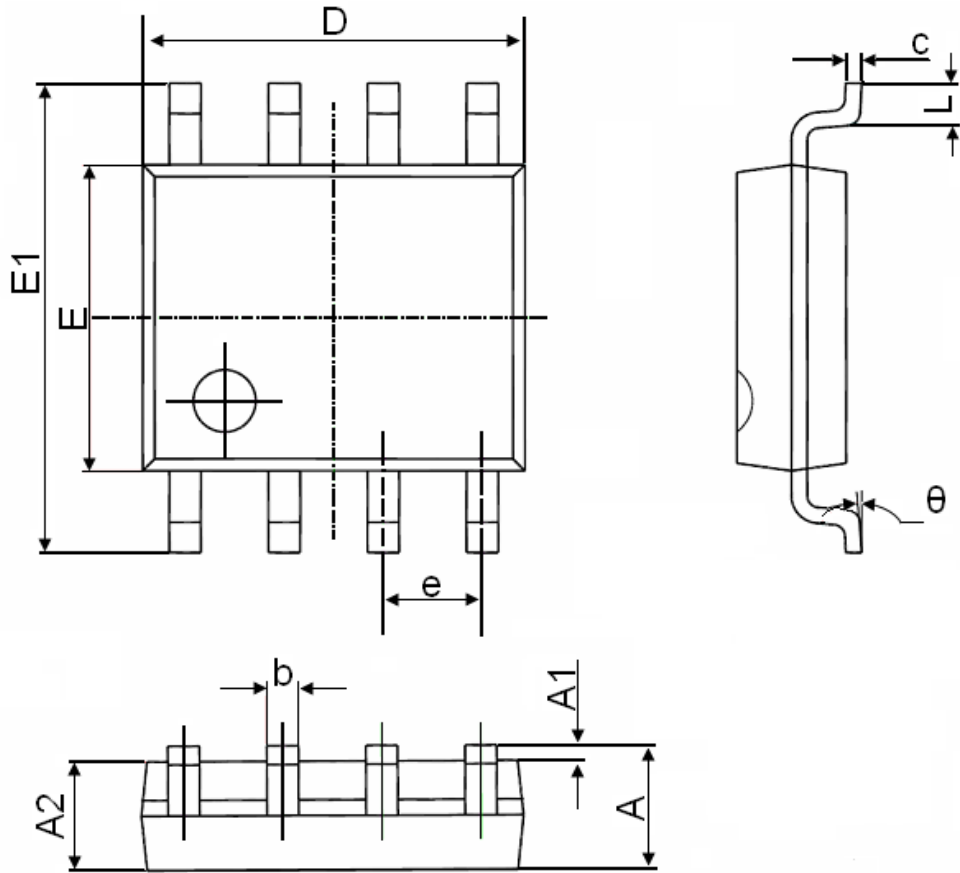


**Figure 13 Safe Operation Area**



**Figure 14 Normalized Maximum Transient Thermal Impedance**

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°