



# 18N25

## Power MOSFET

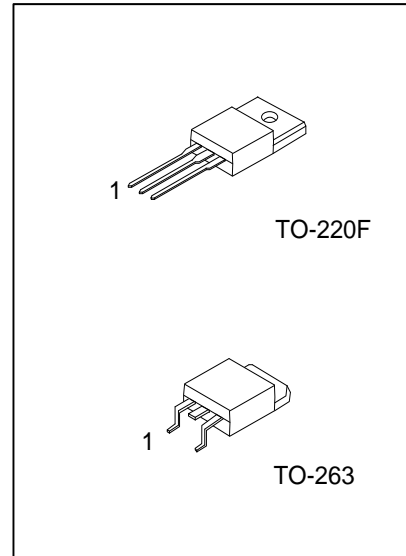
### 18A, 250V N-CHANNEL POWER MOSFET

#### DESCRIPTION

The UTC **18N25** is an N-channel enhancement mode power MOSFET using UTC's advanced planar stripe and DMOS technology to provide perfect performance.

This technology can withstand high energy pulse in the avalanche and commutation mode. It can provide minimum on-state resistance and high switching speed.

This device is generally applied in active power factor correction and high efficient switched mode power supplies.

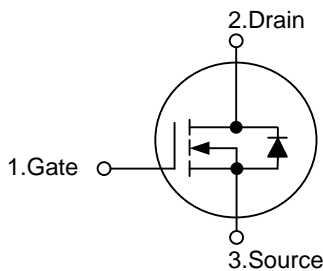


#### FEATURES

\*  $R_{DS(ON)}=0.16\Omega @ V_{GS}=10V$

\* High switching speed

#### SYMBOL



#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
18N25L-TF3-T	18N25G-TF3-T	TO-220F	G	D	S	Tube
18N25L-TQ2-T	18N25G-TQ2-T	TO-263	G	D	S	Tube
18N25L-TQ2-R	18N25G-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>18N25L-TA3-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Lead Free</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TF3: TO-220F, TQ2: TO-263</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATINGS (TC=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage		$V_{DSS}$	250	V
Gate to Source Voltage		$V_{GSS}$	±20	V
Drain Current	Continuous	$I_D$	18	A
	Pulsed (Note 2)	$I_{DM}$	72	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	945	mJ
Avalanche Current (Note 2)		$I_{AR}$	18	A
Power Dissipation	TO-220F	$P_D$	40	W
	TO-263		138	°C
Junction Temperature		$T_J$	+150	°C
Storage Temperature		$T_{STG}$	-55 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. Starting  $T_J=25^\circ\text{C}$ ,  $L=5.2\text{mH}$ ,  $I_{AS}=18\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ .
4. Drain current limited by maximum junction temperature.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		$\theta_{JA}$	62.5	°C/W
Junction to Case	TO-220F	$\theta_{JC}$	3.1	°C/W
	TO-263		0.9	°C/W

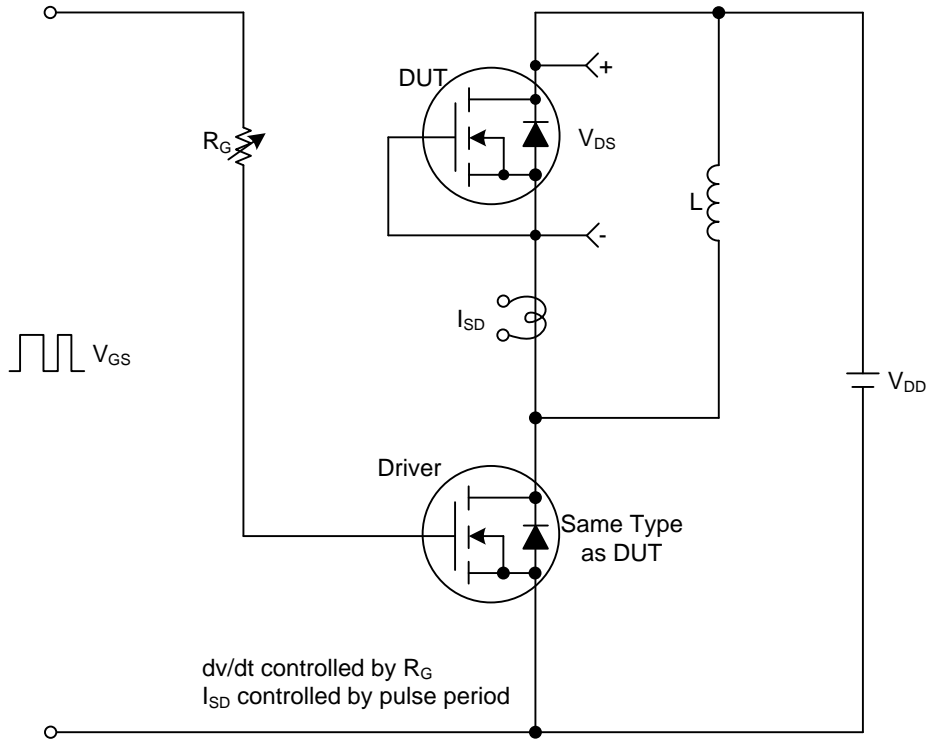
■ ELECTRICAL CHARACTERISTICS (TC=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>							
Drain-Source Breakdown Voltage		$BV_{DSS}$	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	250			V
Drain-Source Leakage Current		$I_{DSS}$	$V_{DS}=250\text{V}$ , $V_{GS}=0\text{V}$			1	$\mu\text{A}$
Gate-Source Leakage Current	Forward	$I_{GSS}$	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$			100	nA
	Reverse		$V_{GS}=-20\text{V}$ , $V_{DS}=0\text{V}$			-100	
<b>ON CHARACTERISTICS</b>							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.0		4.0	V
Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=18\text{A}$		0.16	0.24	$\Omega$
<b>DYNAMIC PARAMETERS</b>							
Input Capacitance		$C_{ISS}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$		2200	2860	pF
Output Capacitance		$C_{OSS}$			330	430	pF
Reverse Transfer Capacitance		$C_{RSS}$			25	40	pF
<b>SWITCHING PARAMETERS</b>							
Total Gate Charge		$Q_G$	$V_{DS}=125\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=18\text{A}$ (Note 1,2)		30	45	nC
Gate-Source Charge		$Q_{GS}$			10		nC
Gate-Drain Charge		$Q_{GD}$			10		nC
Turn-ON Delay Time		$t_{D(ON)}$	$V_{DD}=30\text{V}$ , $I_D=18\text{A}$ , $R_G=25\Omega$ (Note 1,2)		15	25	ns
Turn-ON Rise Time		$t_R$			130	195	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			30	45	ns
Turn-OFF Fall Time		$t_F$			100	150	ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>							
Maximum Body-Diode Continuous Current		$I_S$				18	A
Maximum Body-Diode Pulsed Current		$I_{SM}$				72	A
Drain-Source Diode Forward Voltage		$V_{SD}$	$I_S=18\text{A}$ , $V_{GS}=0\text{V}$			1.4	V

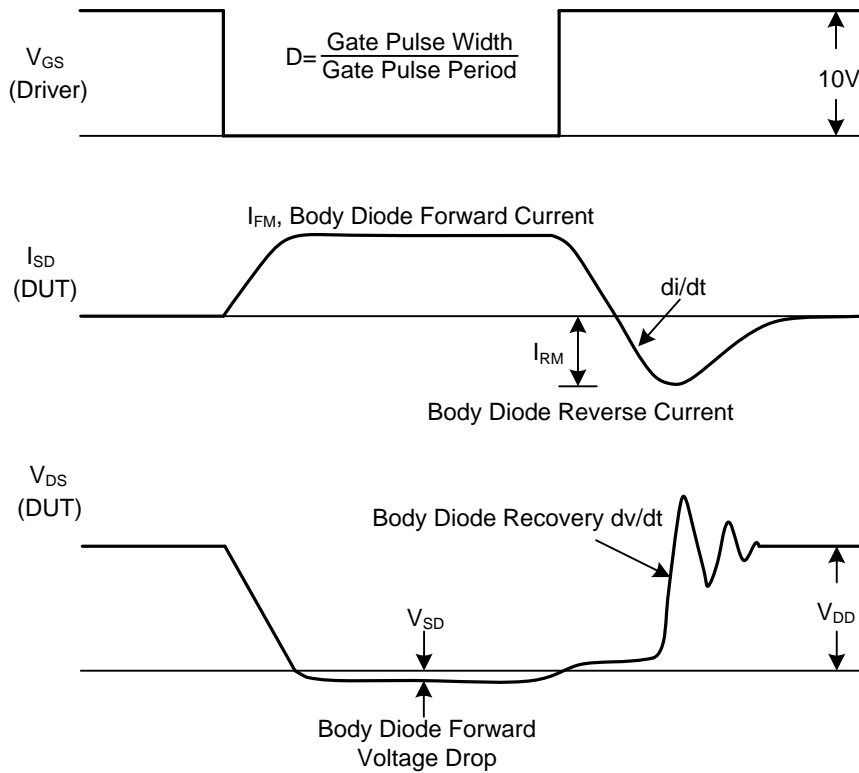
Note: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$ , Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

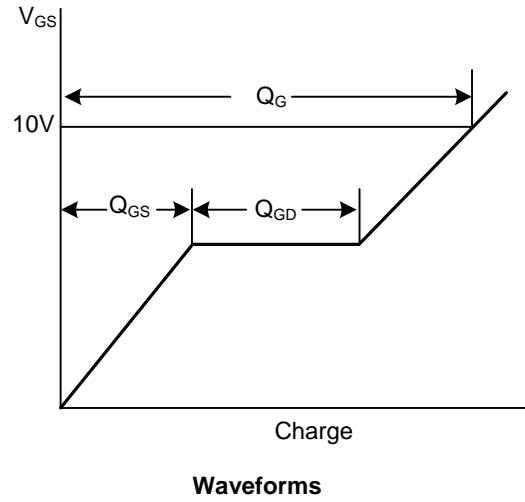
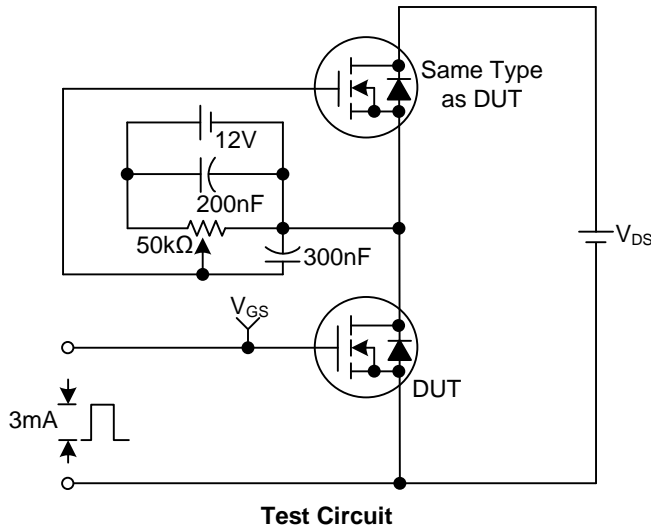


Peak Diode Recovery dv/dt Test Circuit & Waveforms

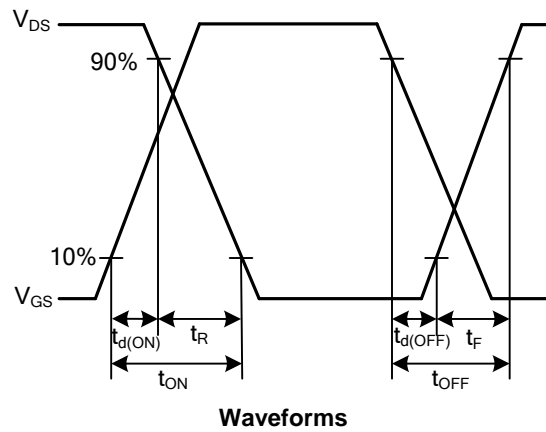
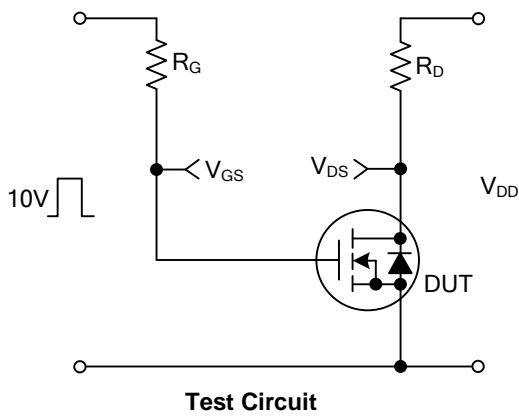


## TEST CIRCUITS AND WAVEFORMS(Cont.)

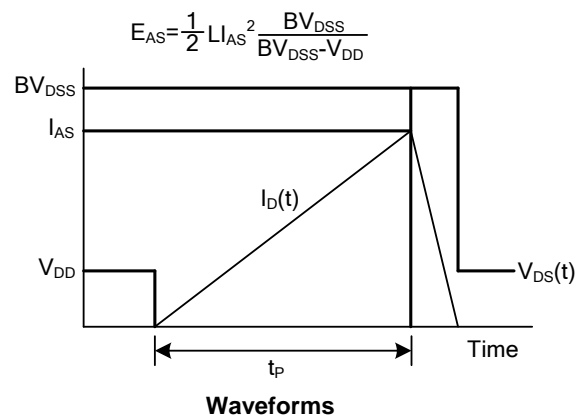
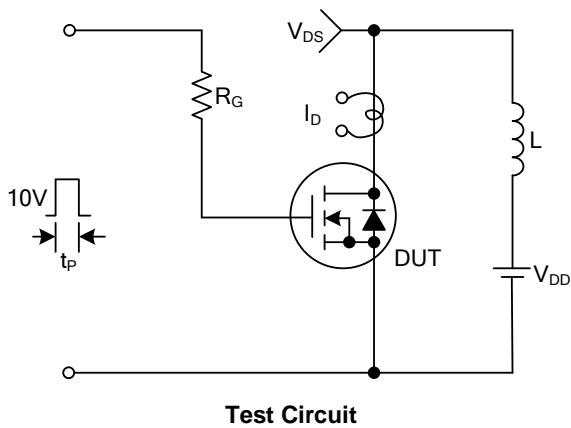
### Gate Charge



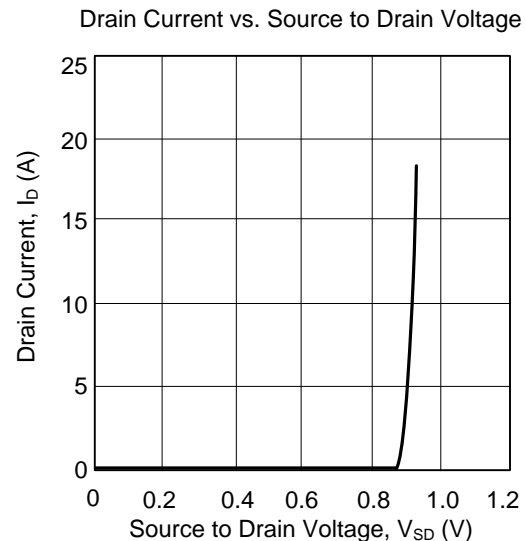
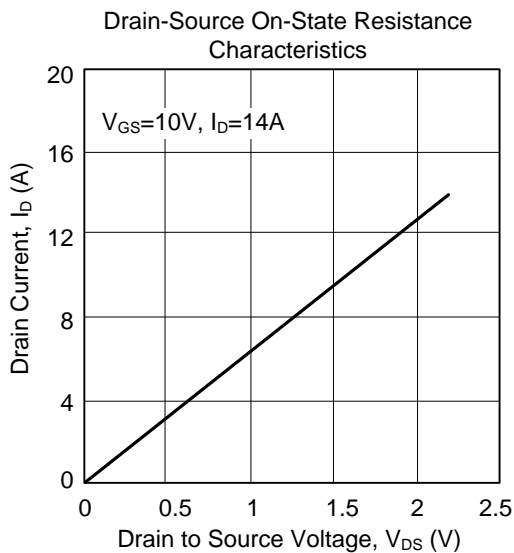
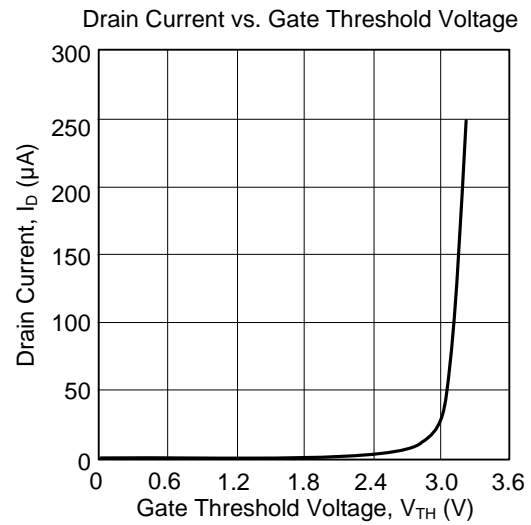
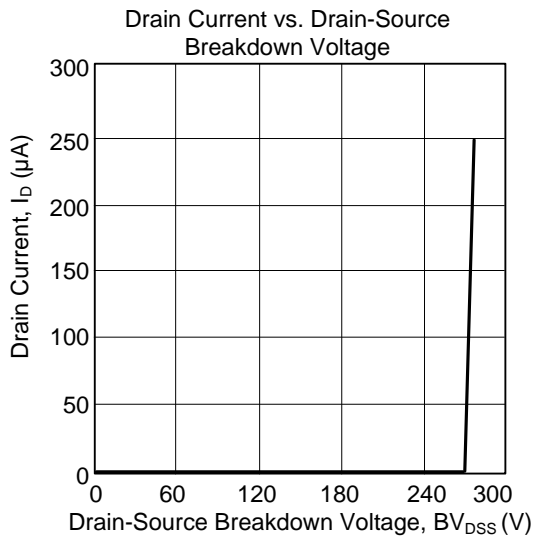
### Resistive Switching



### Unclamped Inductive Switching



## ■ TYPICAL CHARACTERISTICS



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