

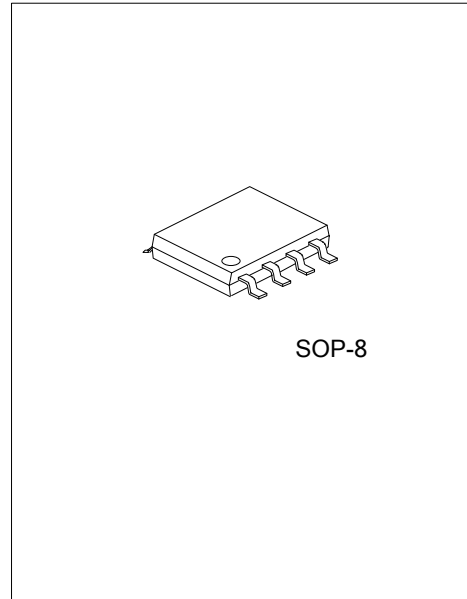


UT4466

Preliminary

Power MOSFET

**10A, 30V N-CHANNEL
ENHANCEMENT MODE
MOSFET**



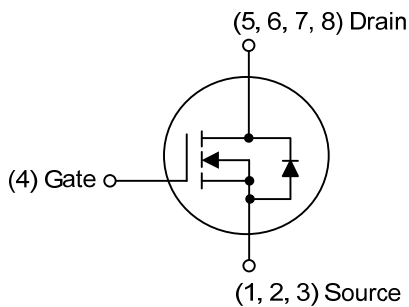
■ DESCRIPTION

The UTC **UT4466** is an N-channel Power FET, it uses UTC's advanced technology to provide customers a minimum on-state resistance, high switching speed and low gate charge.

■ FEATURES

- * $R_{DS(ON)} < 15m\Omega @ V_{GS}=10V, I_D=10A$
- * High switching speed
- * Low gate charge (Typ.=10.5nC)

■ SYMBOL



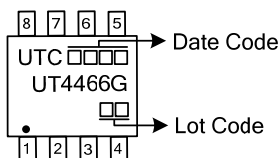
■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UT4466G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

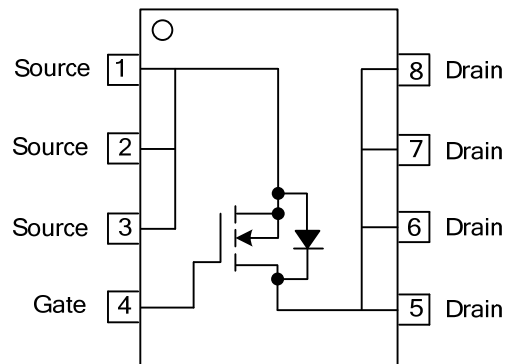
Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT4466G-S08-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free
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■ MARKING



■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V _{DSS}	30	V	
Gate-Source Voltage		V _{GSS}	±25	V	
Drain Current	Continuous(Note 2)	I _D	T _A =25°C	10	A
			T _A =85°C	6	A
Pulsed (Note 3)		I _{DM}	60	A	
Avalanche Current (Note 3, 4)		I _{AR}	16	A	
Repetitive Avalanche Energy (Note 3, 4)		E _{AR}	12.8	mJ	
Power Dissipation (Note 2)		P _D	1.42	W	
Junction Temperature		T _J	-55~+150	°C	
Storage Temperature Range		T _{STG}	-55~+150	°C	

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Device mounted on FR-4 substrate PC board with minimum recommended pad layout in a still air environment @ T_A=25°C. The value in any given application depends on the user's specific board design.
 3. Repetitive rating, pulse width limited by junction temperature.
 4. I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep T_J=25°C

■ THERMAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

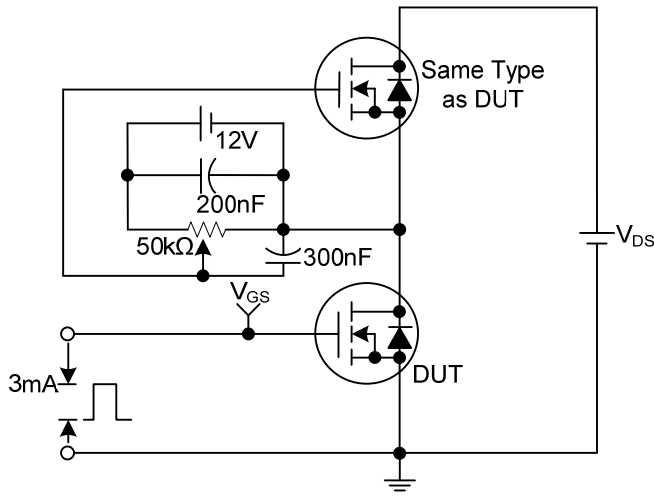
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1)	θ _{JA}	88.4	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

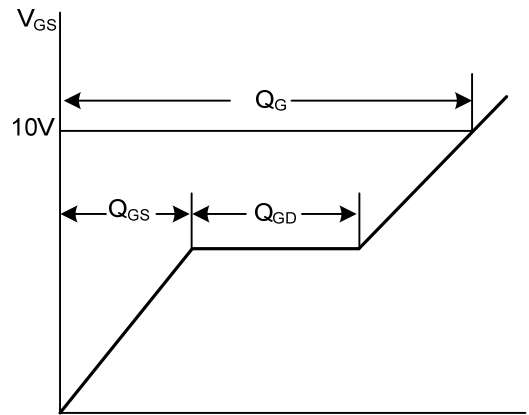
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS (Note 1)						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	30			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =+25V, V _{DS} =0V			+100	nA
		V _{GS} =-25V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS (Note 1)						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.45	2.4	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A		15	23	mΩ
		V _{GS} =4.5V, I _D =7.5A		25	33	mΩ
Forward Transfer Admittance	Y _{FS}	V _{DS} =5V, I _D =10A		2.5		S
DYNAMIC PARAMETERS (Note 2)						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =15V, f=1.0MHz		478.9		pF
Output Capacitance	C _{OSS}			96.7		pF
Reverse Transfer Capacitance	C _{RSS}			61.4		pF
SWITCHING PARAMETERS						
Gate Resistance	R _G	V _{DS} =0V, V _{GS} =0V, f=1MHz	0.4	1.1	1.6	Ω
Total Gate Charge	Q _G	V _{GS} =4.5V, V _{DS} =15V, I _D =10A		5.0	8	nC
Total Gate Charge	Q _G	V _{GS} =10V, V _{DS} =15V, I _D =10A		10.5	17	nC
Gate to Source Charge	Q _{GS}			1.8		nC
Gate to Drain Charge	Q _{GD}			1.6		nC
Turn-ON Delay Time	t _{D(ON)}			2.9		ns
Rise Time	t _R	V _{DS} =15V, V _{GS} =10V, R _G =3Ω,		7.9		ns
Turn-OFF Delay Time	t _{D(OFF)}	R _L =1.5Ω		14.6		ns
Fall-Time	t _F			3.1		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V		0.69	1	V

- Notes: 1. Short duration pulse test used to minimize self-heating effect.
 2. Guaranteed by design. Not subject to production testing.

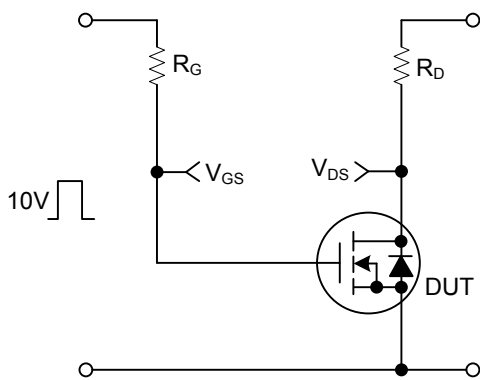
■ TEST CIRCUITS AND WAVEFORMS



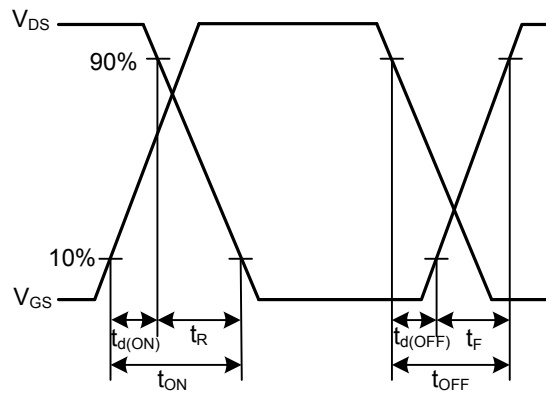
Gate Charge Test Circuit



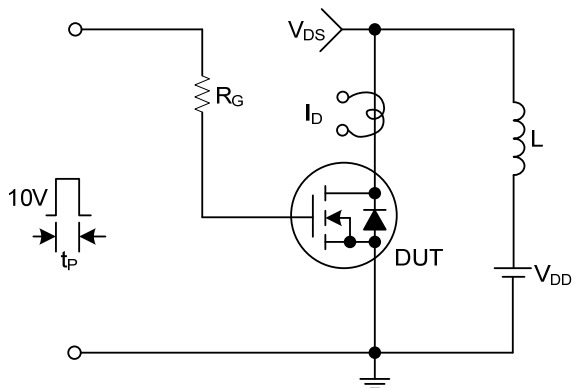
Gate Charge Waveforms



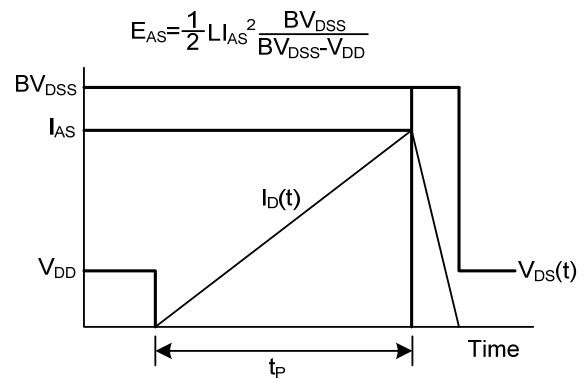
Resistive Switching Test Circuit



Resistive Switching Waveforms



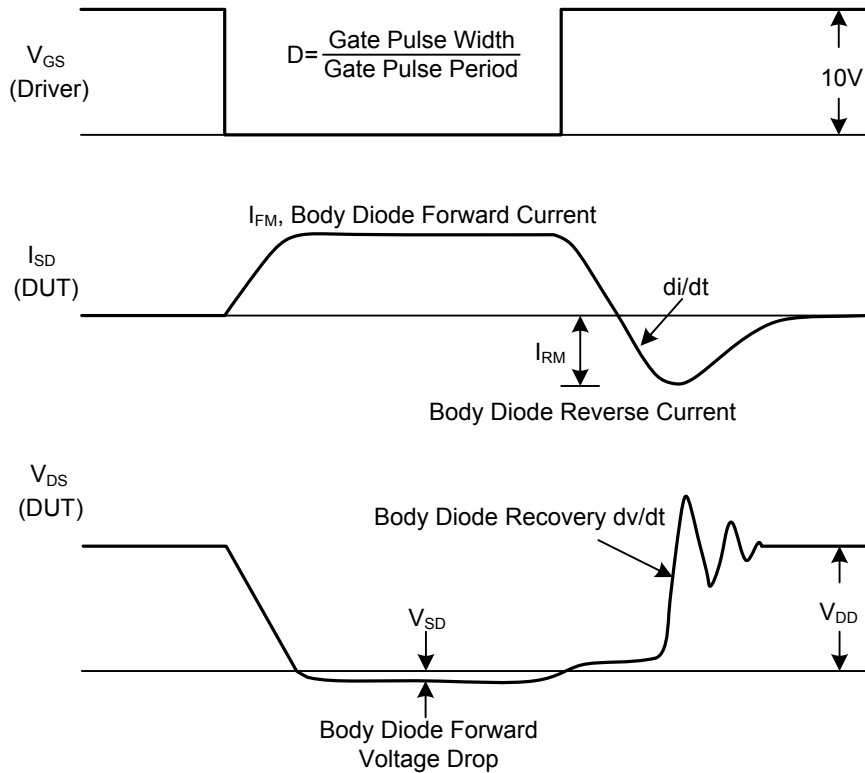
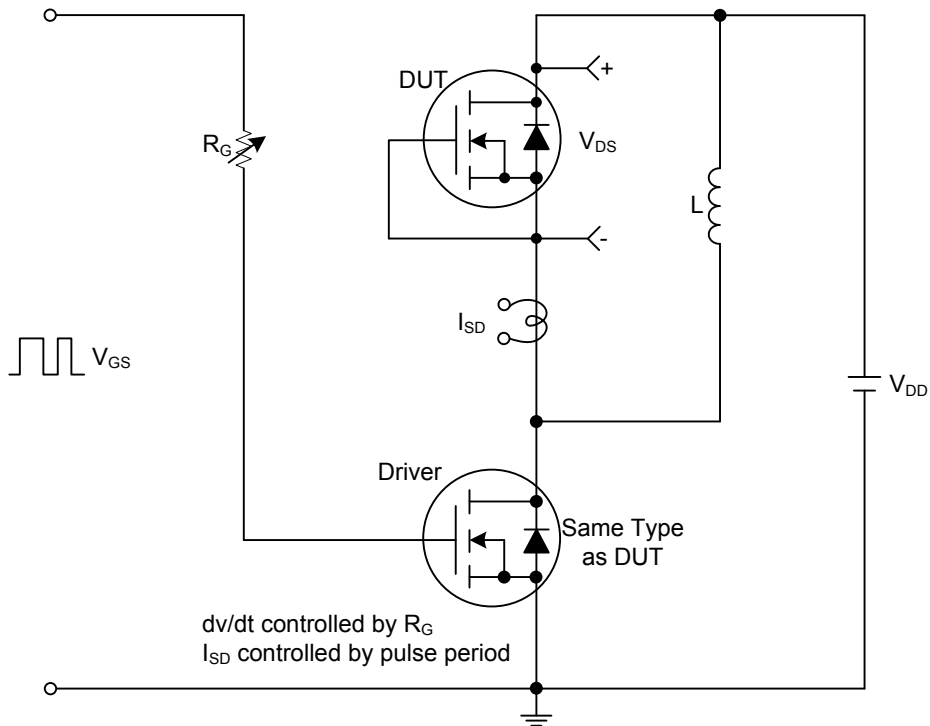
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit and Waveforms

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