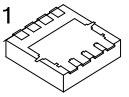
30V, 24A N-CHANNEL ENHANCEMENT MODE POWER MOSFET



DFN-8(3x3)

■ DESCRIPTION

The UTC **UT7410** is an N-channel enhancement MOSFET, it uses UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$ and low gate charge.

The UTC **UT7410** is suitable for Load Switch and DC-DC converters applications, etc.

■ FEATURES

* $R_{DS(ON)}$ < 24mΩ @ V_{GS}=10V, I_D=8A
  $R_{DS(ON)}$ < 32mΩ @ V_{GS}=4.5V, I_D=7A
* Low Gate Charge (typical 9.8nC)

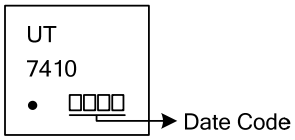
■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UT7410G-K08-3030-R	DFN-8(3×3)	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT7410G-K08-3030-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) K08-3030: DFN-8(3×3) (3) G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise noted)

PARAMETER				SYMBOL	RATINGS	UNIT
Drain-Source Voltage				V_{DSS}	30	V
Gate-Source Voltage				V_{GSS}	±20	V
Drain Current	Continuous	(Note 2)	T_C=25°C	I_D	24	A
			T_C=100°C		15	A
		(Note 1)	T_A=25°C	I_{DSM}	9.5	A
			T_A=70°C		7.7	A
	Pulsed (Note 3)			I_{DM}	40	A
Power Dissipation		(Note 2)	T_C=25°C	P_D	20	W
			T_C=100°C		8.3	W
		(Note 1)	T_A=25°C	P_{DSM}	3.1	W
			T_A=70°C		2	W
Junction Temperature				T_J	-55~+150	°C
Storage Temperature Range				T_{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Junction to Ambient (Note 1)	t≤10s	θ_{JA}		30	40	°C/W
	Steady-State			60	75	°C/W
Junction to Case (Note 2)	Steady-State	θ_{JC}		5	6	°C/W

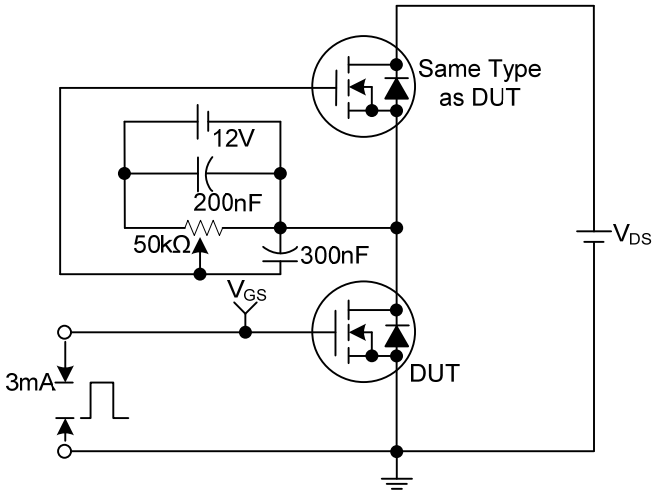
Notes: 1. The value of θ_{JA} is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on θ_{JA} t≤10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

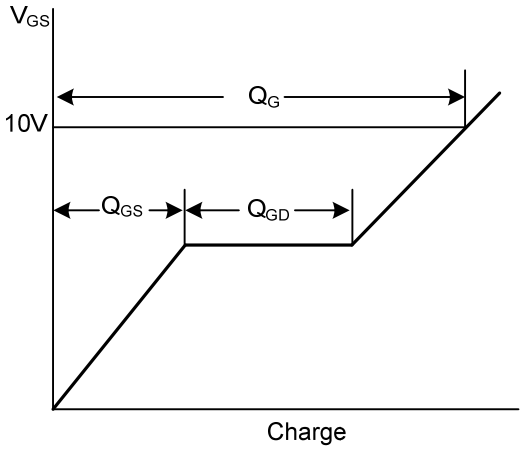
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.4	1.8	2.5	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=8A		18	24	mΩ
			V_{GS}=4.5V, I_D=7A		27	32	mΩ
Forward Transconductance		g_{FS}	V_{DS}=5V, I_D=8A		30		S
On State Drain Current		$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	40			A
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=15V, f=1.0MHz		550		pF
Output Capacitance		C_{OSS}			110		pF
Reverse Transfer Capacitance		C_{RSS}			55		pF
Gate resistance		R_G	V_{GS}=0V, V_{DS}=0V, f=1.0MHz		4	4.9	Ω
SWITCHING PARAMETERS							
Total Gate Charge	10V	Q_G	V_{GS}=10V, V_{DS}=15V, I_D=8A		9.8		nC
	4.5V				4.6		nC
Gate to Source Charge		Q_{GS}			1.8		nC
Gate to Drain Charge		Q_{GD}			2.2		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{GS}=10V, V_{DS}=15V, R_L=2Ω, R_{GEN}=3Ω		5		ns
Rise Time		t_R			3.2		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			24		ns
Fall-Time		t_F			6		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				1.7	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=1A, V_{GS}=0V		0.75	1	V

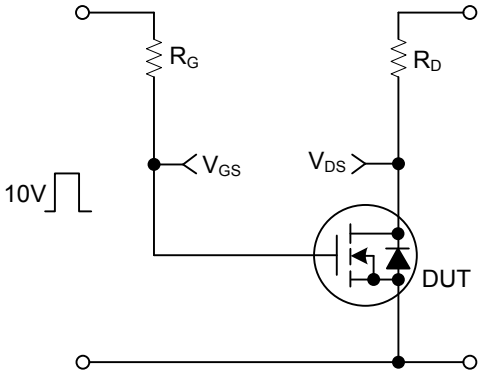
■ TEST CIRCUITS AND WAVEFORMS



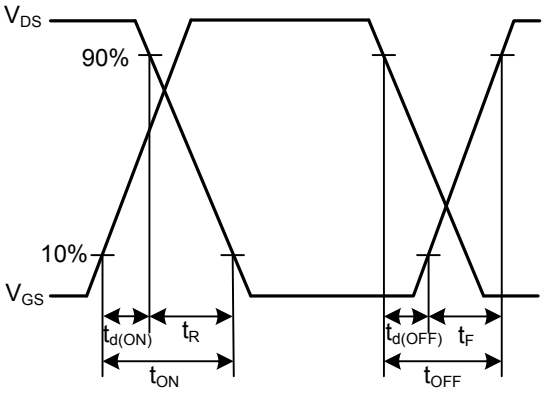
Gate Charge Test Circuit



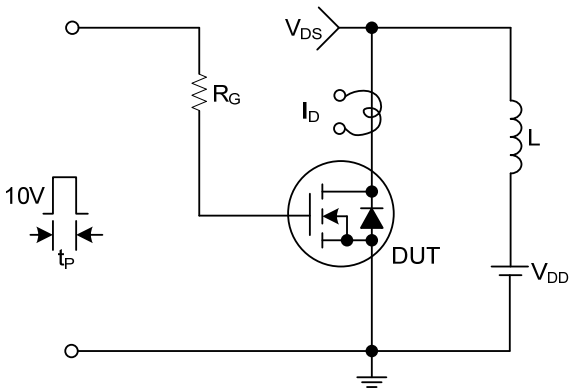
Gate Charge Waveforms



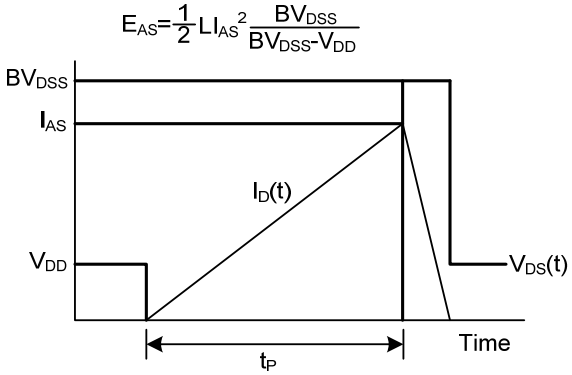
Resistive Switching Test Circuit



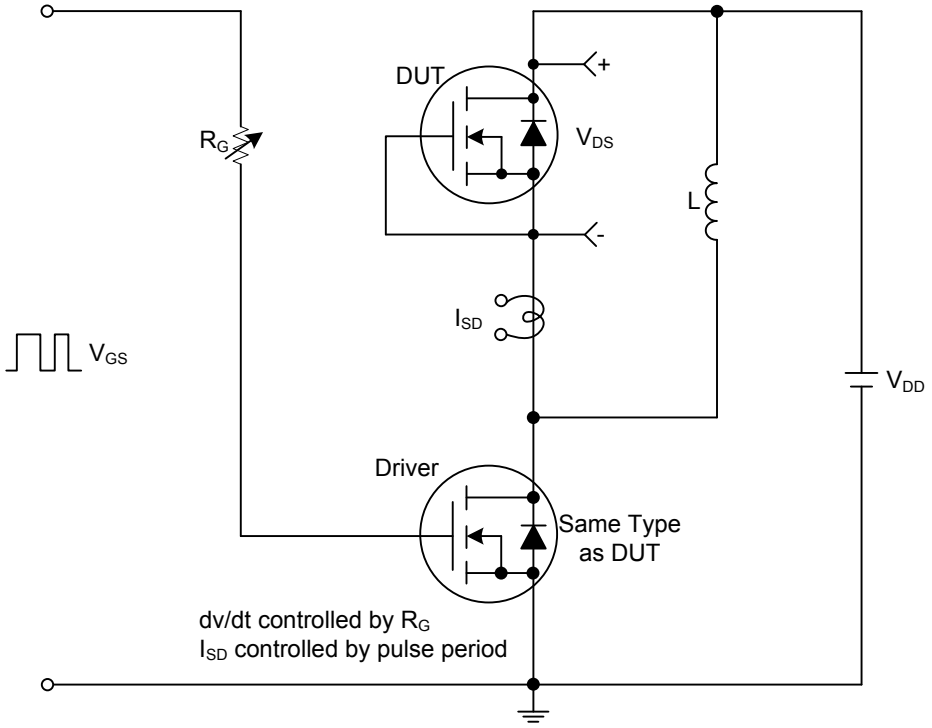
Resistive Switching Waveforms

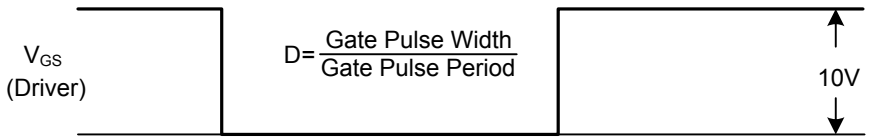


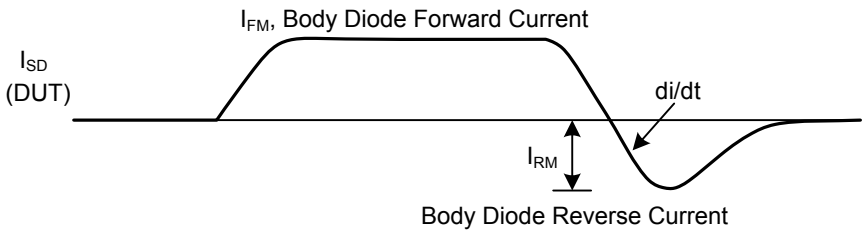
Unclamped Inductive Switching Test Circuit

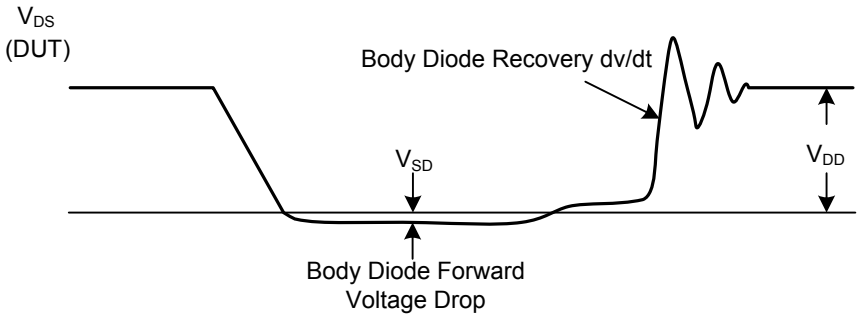


Unclamped Inductive Switching Waveforms









Peak Diode Recovery dv/dt Test Circuit and Waveforms