



19N10V

Power MOSFET

100V N-Channel MOSFET

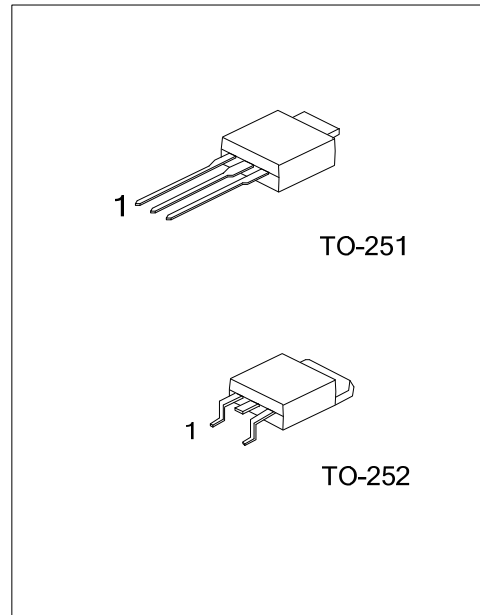
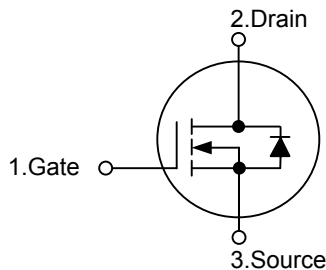
DESCRIPTION

The UTC 100V N-Channel enhancement mode power field effect transistors (MOSFET) are produced by UTC's planar stripe, DMOS technology which has been tailored especially in the avalanche and commutation mode to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse. They are suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

FEATURES

- * $R_{DS(ON)} = 0.1\Omega @ V_{GS} = 10V$
- * Ultra low gate charge (typical 19nC)
- * Low reverse transfer Capacitance ($C_{RSS} =$ typical 32pF)
- * Fast switching capability
- * Avalanche energy Specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
19N10VL-TM3-T	19N10VG-TM3-T	TO-251	G	D	S	Tube
19N10VL-TN3-R	19N10VG-TN3-R	TO-252	G	D	S	Tape Reel

<p>19N10VL-TM3-T</p>	<p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) TM3: TO-251, TN3: TO-252 (3) L: Lead Free, G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V _{DSS}	100	V
Gate-Source Voltage	V _{GSS}	± 25	V
Continuous Drain Current	I _D	15.6	A
Pulsed Drain Current (Note 2)	I _{DM}	62.4	A
Avalanche Current (Note 2)	I _{AR}	15.6	A
Single Pulsed Avalanche Energy (Note 3)	E _{AS}	220	mJ
Repetitive Avalanche Energy (Note 2)	E _{AR}	5.0	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	6.0	V/ns
Power Dissipation	P _D	50	W
Junction Temperature	T _J	+150	°C
Storage Temperature	T _{STG}	-55 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by T_{J(MAX)}

3. L=1.35mH, I_{AS}=15.6A, V_{DD}=25V, R_G=25 Ω, Starting T_J=25°C

4. I_{SD}≤19A, di/dt ≤ 300A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ _{JA}	50	°C/W
Junction to Case	θ _{JC}	2.5	°C/W

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C		0.1		V/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =25V, V _{DS} =0V			100	nA
		V _{GS} =-25V, V _{DS} =0V			-100	
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =7.8A		0.078	0.1	Ω
Forward Transconductance	g _{FS}	V _{DS} =40V, I _D =7.8A (Note 1)			11	S
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		600	780	pF
Output Capacitance	C _{OSS}			165	215	pF
Reverse Transfer Capacitance	C _{RSS}			32	40	pF

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=80V, I_D=19A, V_{GS}=10V$ (Note 1, 2)		19	25	nC
Gate Source Charge	Q_{GS}			3.9		
Gate Drain Charge	Q_{GD}			9.0		
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=50V, I_D=19A, R_G=25\Omega$ (Note 1, 2)		7.5	25	ns
Turn-ON Rise Time	t_R			150	310	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			20	50	ns
Turn-OFF Fall-Time	t_F			65	140	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=15.6A$			1.5	V
Maximum Body-Diode Continuous Current	I_S				15.6	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				62.4	A
Body Diode Reverse Recovery Time	t_{RR}	$V_{GS}=0V, I_S=19A,$ $dI_F/dt=100A/\mu s$ (Note 1)		78		ns
Body Diode Reverse Recovery Charge	Q_{RR}			200		nC

Note: 1. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

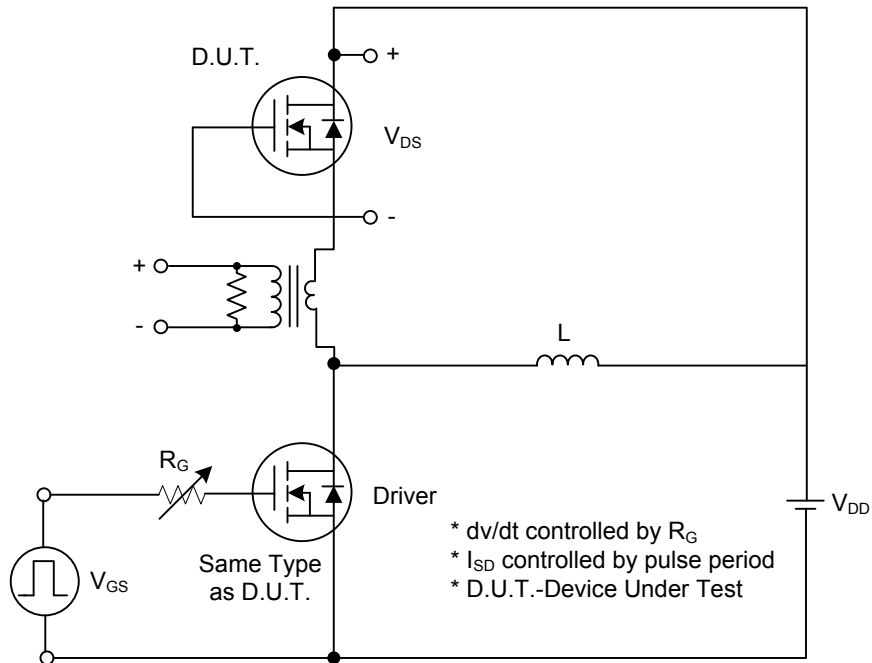


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

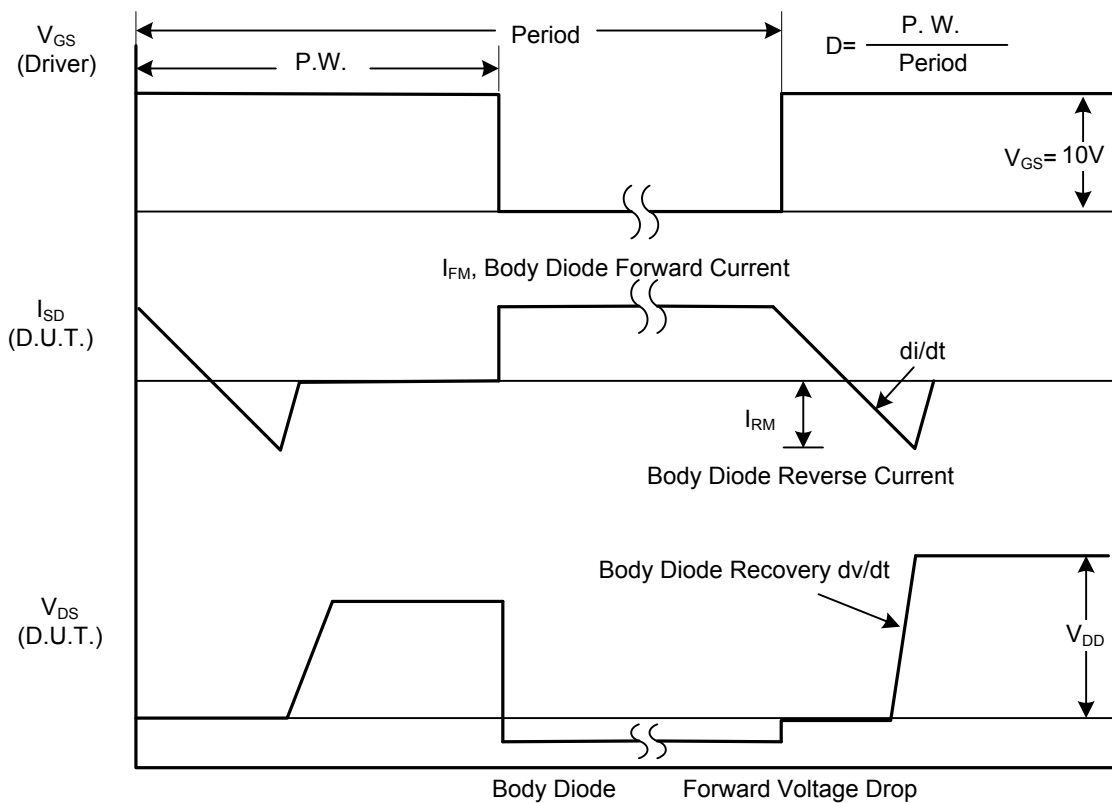


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

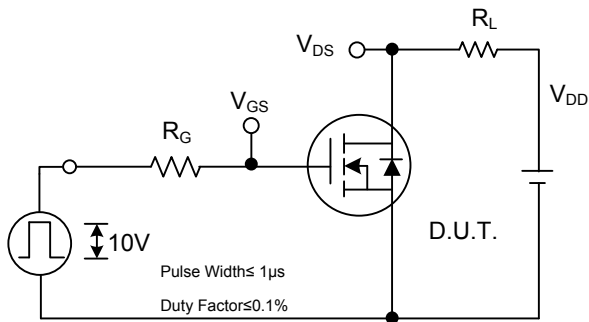


Fig. 2A Switching Test Circuit

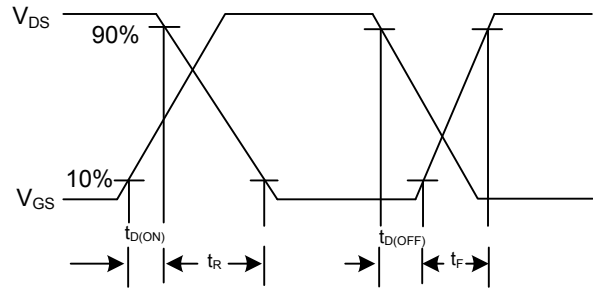


Fig. 2B Switching Waveforms

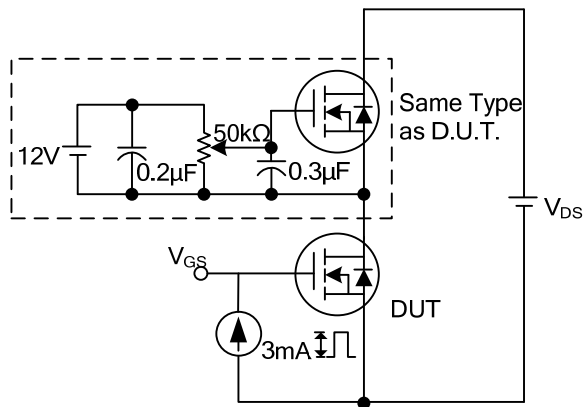


Fig. 3A Gate Charge Test Circuit

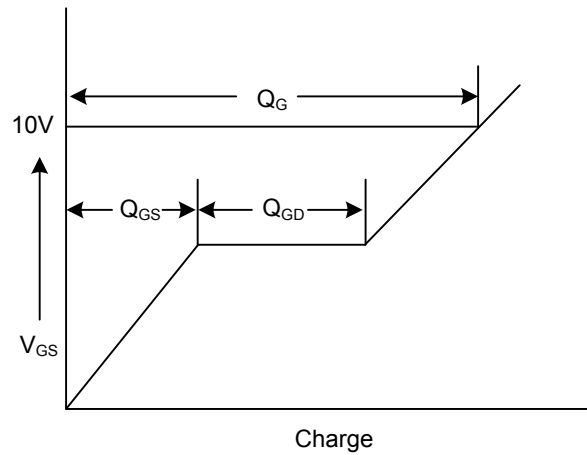


Fig. 3B Gate Charge Waveform

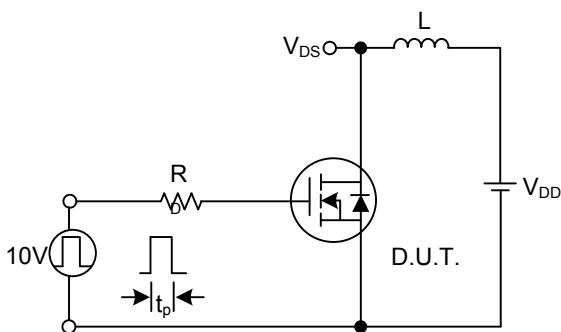


Fig. 4A Unclamped Inductive Switching Test Circuit

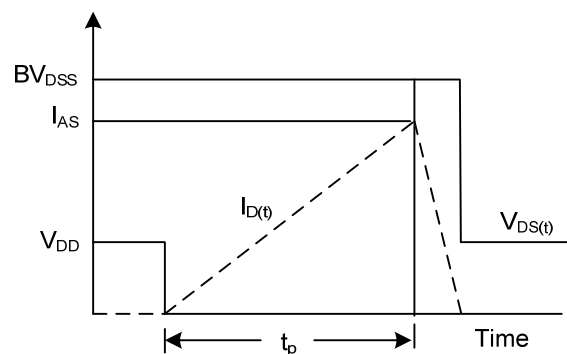
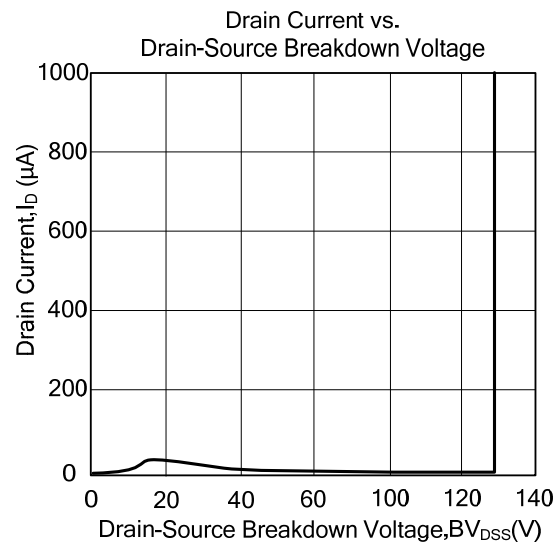
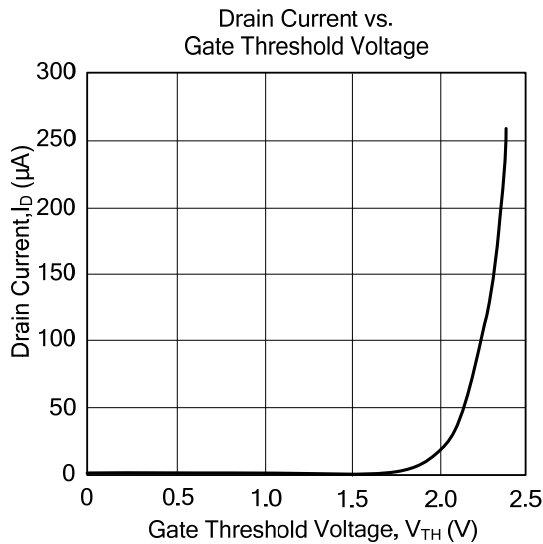
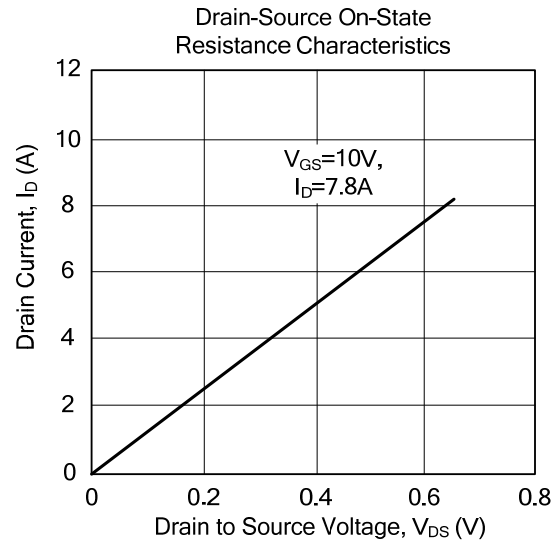
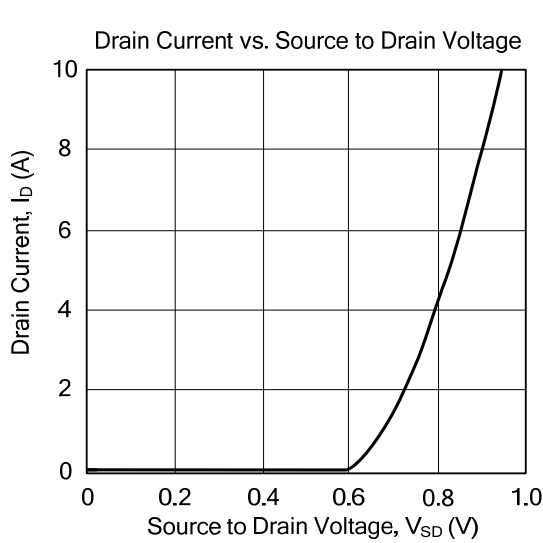


Fig. 4B Unclamped Inductive Switching Waveforms

TYPICAL CHARACTERISTICS



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