



UF640-P

Power MOSFET

18A, 200V, 0.18OHM, N-CHANNEL POWER MOSFET

DESCRIPTION

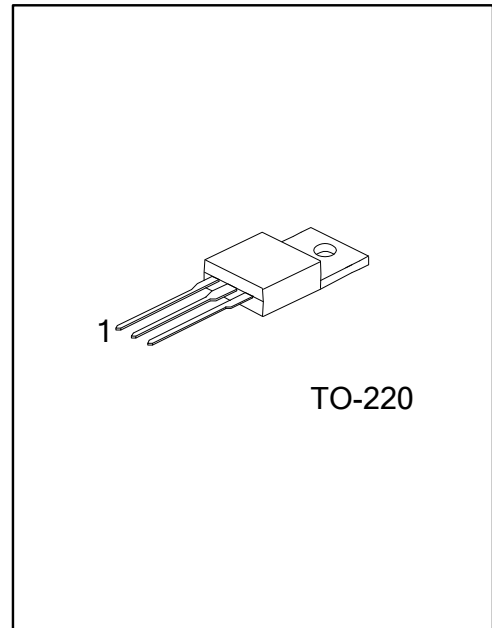
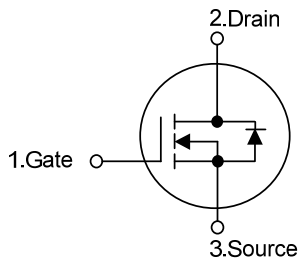
These kinds of n-channel power MOSFET field effect transistor have low conduction power loss, high input impedance, and high switching speed, Linear Transfer Characteristics, so can be use in a variety of power conversion applications.

The **UF640-P** suitable for resonant and PWM converter topologies.

FEATURES

- * $R_{DS(ON)}=0.18\Omega @ V_{GS}=10V, I_D=10A$
- * Ultra Low gate charge (typical 43nC)
- * Low reverse transfer capacitance ($C_{RSS} = \text{typical } 100 \text{ pF}$)
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
UF640L-TA3-T	UF640G-TA3-T	TO-220	G	D	S	Tube

<p>UF640L-TA3-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) T: Tube (2) TA3: TO-220 (3) L: Lead Free, G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATING ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	200	V
Drain-Gate Voltage ($R_{GS}=20\text{k}\Omega$)	V_{DGR}	200	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current	I_D	18	A
Pulsed Drain Current (Note 2)	I_{DM}	72	A
Single Pulse Avalanche Energy Rating (Note 2)	E_{AS}	580	mJ
Maximum Power Dissipation	P_D	123	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

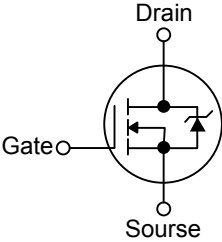
2. $L=3.37\text{mH}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, peak $I_{AS}=18\text{A}$, starting $T_J=25^\circ\text{C}$.

3. Pulse width limited by $T_{J(MAX)}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C/W}$
Junction to Case	θ_{JC}	1.01	$^\circ\text{C/W}$

■ ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	200			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V			25	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(THR)}	V _{GS} =V _{DS} , I _D =250μA	2		4	V
Drain-Source On Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A		0.13	0.17	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1MHz		805		pF
Output Capacitance	C _{OSS}			240		pF
Reverse Transfer Capacitance	C _{RSS}			46		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =100V, I _D ≈18A, R _G =9.1Ω, R _L =5.4Ω, MOSFET Switching Times are Essentially Independent of Operating Temperature		26	40	ns
Turn-ON Rise Time	t _R			46	70	ns
Turn-OFF Delay Time	t _{D(OFF)}			300	350	ns
Turn-OFF Fall-Time	t _F			97	120	ns
Total Gate Charge	Q _{G(TOT)}	V _{GS} =10V, I _D ≈18A, V _{DS} =0.8 x Rated BV _{DSS} Gate Charge is Essentially Independent of Operating Temperature I _{G(REF)} = 1.5mA		34	55	nC
Gate Source Charge	Q _{GS}			5.5		nC
Gate Drain Charge	Q _{GD}			6.6		nC
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Diode Forward Voltage (Note)	V _{SD}	T _J =25°C, I _S =18A, V _{GS} =0V,			2.0	V
Continuous Source Current (body diode)	I _S	Integral Reverse p-n Junction Diode in the MOSFET			18	A
Pulse Source Current (body diode) (Note)	I _{SM}					72
Reverse Recovery Time	t _{rr}	T _J =25°C, I _S =18A, dI _S /dt=100A/μs	120	240	530	ns
Reverse Recovery Charge	Q _{RR}	T _J =25°C, I _S =18A, dI _S /dt=100A/μs	1.3	2.8	5.6	μC

Note: Pulse Test: Pulse width ≤ 300μs, duty cycle ≤ 2%.

■ TEST CIRCUIT

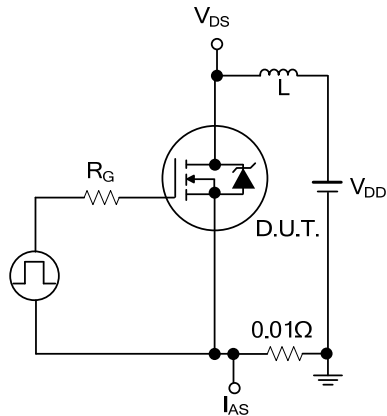


Fig. 1 Unclamped Energy Test Circuit

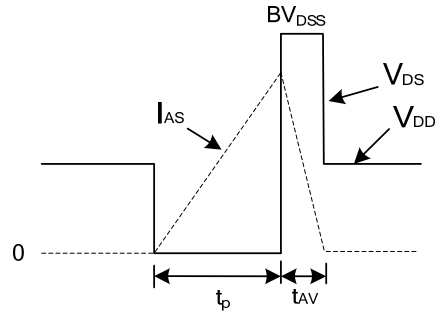


Fig.2 Unclamped Energy Waveforms

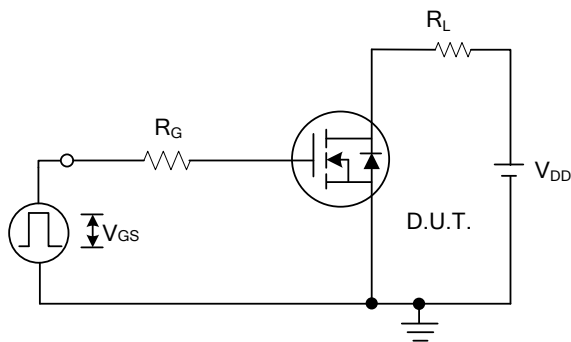


Fig.3 Switching Time Test Circuit

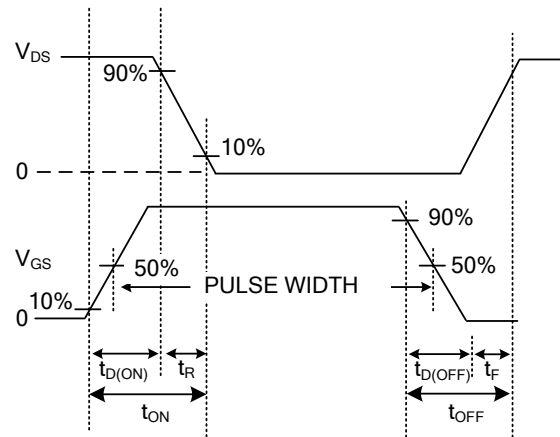


Fig.4 Resistive Switching Waveforms

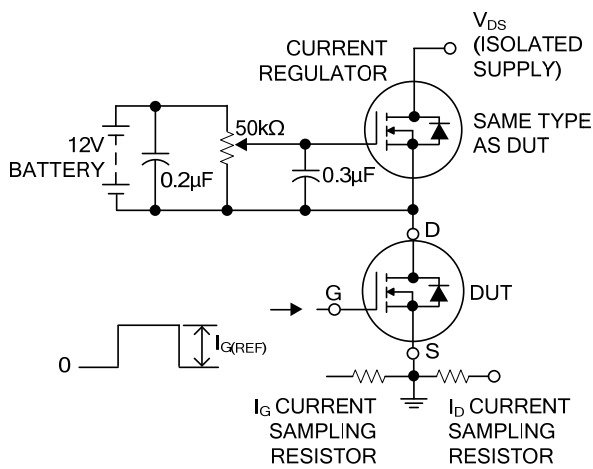


Fig.5 Gate Charge Test Circuit

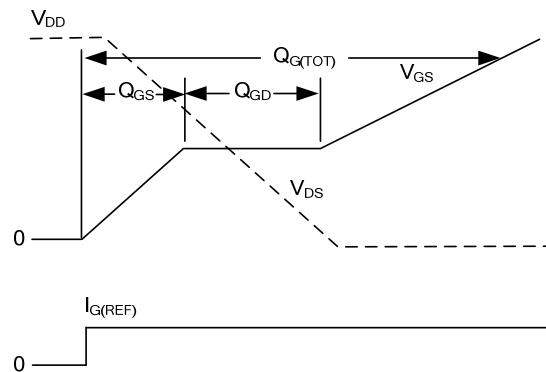


Fig.6 Gate Charge Waveforms

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