# UNISONIC TECHNOLOGIES CO., LTD

25N20 **Power MOSFET** 

# 25A, 200V N-CHANNEL **ENHANCEMENT MODE POWER MOSFET**

#### **DESCRIPTION**

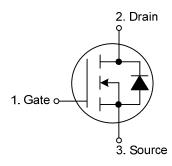
The UTC 25N20 is an N-channel enhancement mode power MOSFET and it uses UTC's perfect technology to provide designers with fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

It is generally suitable for all commercial-industrial applications and DC/DC converters requiring low voltage.

#### **FEATURES**

- \*  $R_{DS(ON)}$  < 160 m $\Omega$  @  $V_{GS}$  =10V,  $I_{D}$  =16A
- \* Single Drive Requirement
- \* Low Gate Charge
- \* RoHS Compliant

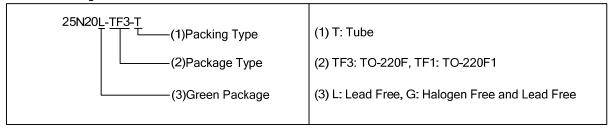
#### **SYMBOL**



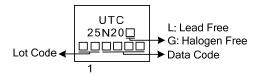
## **ORDERING INFORMATION**

Ordering Number		Dookogo	Pin Assignment			Dooking	
Lead Free	Halogen Free	Package	1	2	3	Packing	
25N20L-TF3-T	25N20G-TF3-T	TO-220F	G	D	S	Tube	
25N20L-TF1-T	25N20G-TF1-T	TO-220F1	G	D	S	Tube	

Note: Pin Assignment: G: Gate S: Source D: Drain



#### **MARKING**



TO-220F TO-220F1

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#### ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain Source Voltage		$V_{DSS}$	200	V	
Gate Source Voltage		$V_{GSS}$	±20	V	
Continuous Drain Current	T <sub>C</sub> =25°C	I <sub>D</sub>	25	Α	
(V <sub>GS</sub> =10V)	T <sub>C</sub> = 100°C	I <sub>D</sub>	15.86	Α	
Pulsed Drain Current (Note 2)		I <sub>DM</sub>	80	Α	
Total Power Dissipation (T <sub>C</sub> =25°C)		P <sub>D</sub>	50	W	
Operating Junction Temperature		TJ	-55 ~ +150	°C	
Storage Temperature		T <sub>STG</sub>	-55 ~ <b>+</b> 150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

#### **■ THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT		
Junction to Ambient	$\theta_{JA}$	62.5	°C/W		
Junction to Case	$\theta_{ m JC}$	2.5	°C/W		

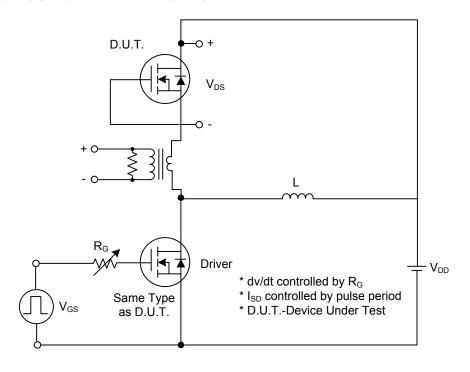
## ■ **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
OFF CHARACTERISTICS				ā.					
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250 \mu A$	200			V			
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_{J}$	Reference to 25°C , I <sub>D</sub> =1mA		0.14		V/°C			
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C V <sub>DS</sub> =80V, V <sub>GS</sub> =0V,T <sub>J</sub> =150°C			1 100	μA μA			
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V			±100	nA			
ON CHARACTERISTICS									
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	2		4	V			
Static Drain-Source On-Resistance (Note)	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =16A		112	160	mΩ			
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =10V, I <sub>D</sub> =16A		14		S			
DYNAMIC PARAMETERS									
Input Capacitance	C <sub>ISS</sub>			1000	1700	pF			
Output Capacitance	Coss	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz		240		рF			
Reverse Transfer Capacitance	$C_{RSS}$	7		25		pF			
SWITCHING PARAMETERS									
Turn-ON Delay Time <sup>1</sup>	$t_{D(ON)}$			56		ns			
Turn-ON Rise Time	$t_R$	$V_{DD}$ =30V, $I_{D}$ =0.5A, $R_{G}$ =25m $\Omega$ ,		75		ns			
Turn-OFF Delay Time	t <sub>D(OFF)</sub>	$V_{GS}$ =10V, $R_{D}$ =3.125 $\Omega$		240		ns			
Turn-OFF Fall-Time	$t_{F}$			100		ns			
Total Gate Charge (Note)	$Q_{G}$			35	40	nC			
Gate Source Charge	$Q_{GS}$	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =1.3A		8		nC			
Gate Drain Charge	$Q_GD$			9.7		nC			
SOURCE- DRAIN DIODE RATINGS AND C	HARACTERIS	STICS							
Drain-Source Diode Forward Voltage (Note)	$V_{SD}$	I <sub>S</sub> =25A, V <sub>GS</sub> =0V			1.3	V			
Reverse Recovery Time	t <sub>RR</sub>	I <sub>S</sub> =25A,V <sub>GS</sub> =0V,		90		ns			
Reverse Recovery Charge	$Q_{RR}$	dI/dt=100A/μs		380		nC			

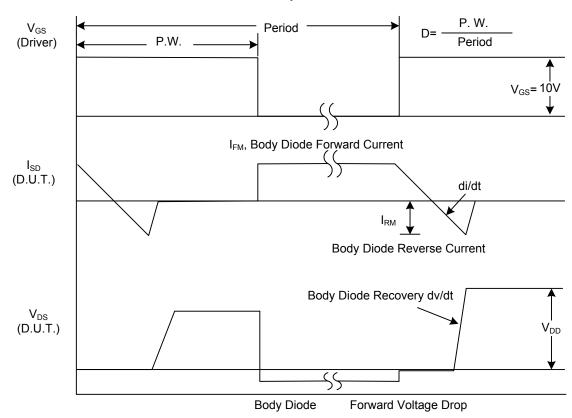
Note: Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%.

<sup>2.</sup> Pulse width limited by max. junction temperature.

#### **■ TEST CIRCUITS AND WAVEFORMS**

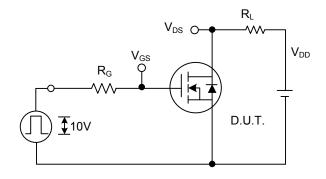


Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

# ■ TEST CIRCUITS AND WAVEFORMS (Cont.)



V<sub>DS</sub> 90%

V<sub>GS</sub> 10%

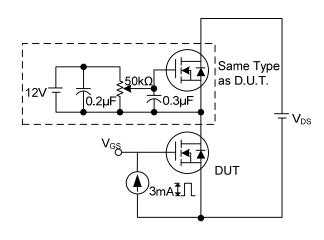
t<sub>D(ON)</sub>

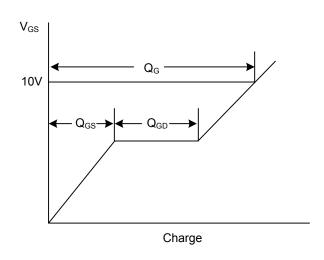
t<sub>R</sub> → |

t<sub>R</sub> + t<sub>F</sub> →

**Switching Test Circuit** 

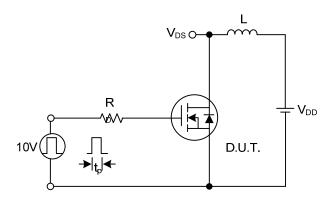
**Switching Waveforms** 

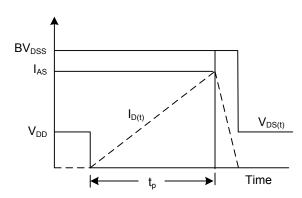




**Gate Charge Test Circuit** 

**Gate Charge Waveform** 

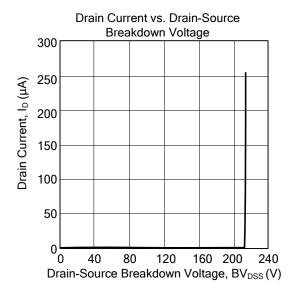


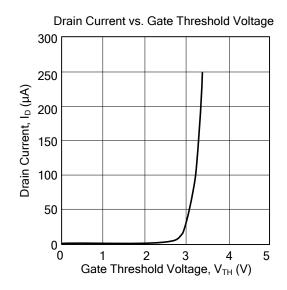


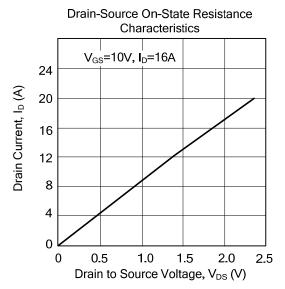
**Unclamped Inductive Switching Test Circuit** 

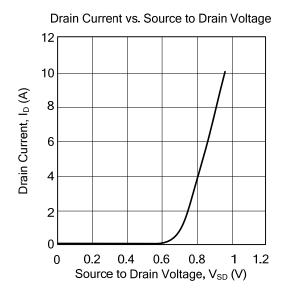
**Unclamped Inductive Switching Waveforms** 

#### **■ TYPICAL CHARACTERISTICS**









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