

UNISONIC TECHNOLOGIES CO., LTD

13N50K-MT **Power MOSFET Preliminary**

13A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

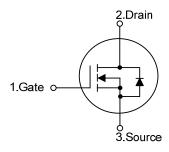
The UTC 13N50K-MT is an N-Channel enhancement mode power MOSFET. The device adopts planar stripe and uses DMOS technology to minimize and provide lower on-state resistance and faster switching speed. It can also withstand high energy pulse under the avalanche and commutation mode conditions.

The UTC 13N50K-MT is ideally suitable for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge topology.



- * $R_{DS(ON)}$ < 0.41 Ω @ V_{GS} = 10V, I_D = 6.5 A
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

SYMBOL

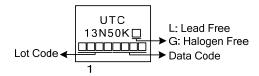


ORDERING INFORMATION

	Ordering Number		Dookogo	Pin Assignment			Dooking	
	Lead Free	Halogen Free	Package	1	2	3	Packing	
	13N50KL-TF2-T	13N50KG-TF2-T	TO-220F2	G	D	S	Tube	
ı	Note: Pin Assignment: G: Ga	te D: Drain S: Source			•			

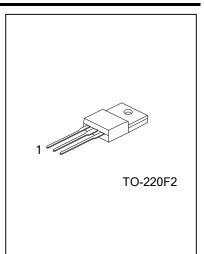
13N50KL-TF2-T (1)Packing Type (1) T: Tube (2)Package Type (2) TF2: TO-220F2 (3) Green Package (3) L: Lead Free, G: Halogen Free and Lead Free

MARKING



www.unisonic.com.tw 1 of 5 QW-R502-B09.d





■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT	
Drain-Source Voltage	V_{DSS}	500	V	
Gate-Source Voltage	V_{GSS}	±30	V	
Continuous Drain Current	I _D	13	Α	
Pulsed Drain Current (Note 2)	I _{DM}	52	Α	
Avalanche Current (Note 2)	I _{AR}	13	Α	
Single Pulsed Avalanche Energy (Note 3)	E _{AS}	625	mJ	
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns	
Power Dissipation (T _C =25°C)	P_{D}	35	W	
Junction Temperature	TJ	+150	°C	
Storage Temperature	T _{STG}	-55~+150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating : Pulse width limited by maximum junction temperature
- 3. L = 7.39mH, I_{AS} = 13A, V_{DD} = 50V, R_{G} = 25 Ω , Starting T_{J} = 25 $^{\circ}$ C
- 4. $I_{SD} \le 13.A$, di/dt $\le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25$ °C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT	
Junction to Ambient	θ_{JA}	62.5	°C/W	
Junction to Case	θ_{JC}	3.58	°C/W	

■ **ELECTRICAL CHARACTERISTICS** (T_C =25°C, unless otherwise specified)

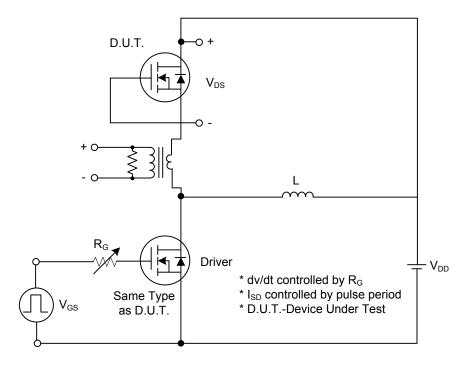
PARAMETER	SYMBOL TEST CONDITIONS		MIN	TYP	MAX	UNIT		
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage	BV _{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	500			V		
Drain-Source Leakage Current	I _{DSS}	$V_{DS} = 500V, V_{GS} = 0V$			10	μΑ		
ata Sauraa Laakaga Currant	I _{GSS}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA		
Gate-Source Leakage Current		$V_{GS} = -30V, V_{DS} = 0V$			-100	nA		
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_{J}$	I _D =250mA,Referenced to 25°C		0.5		V/°C		
ON CHARACTERISTICS	_							
Gate Threshold Voltage	$V_{GS(TH)}$ $V_{DS} = V_{GS}$, $I_D = 250\mu A$		2.0		4.0	V		
Static Drain-Source On-State Resistance	R _{DS(ON)}	$V_{GS} = 10V, I_D = 6.5A$		0.35	0.41	Ω		
DYNAMIC CHARACTERISTICS								
Input Capacitance	C _{ISS})/ OF)/)/ O)/		875		pF		
Output Capacitance	Coss	−V _{DS} =25V, V _{GS} =0V, −f=1.0MHz		177		pF		
Reverse Transfer Capacitance	C _{RSS}			11.5		pF		
SWITCHING CHARACTERISTICS								
Turn-On Delay Time	t _{D(ON)}	V_{DS} =30V, I_{D} =0.5A, R_{G} =25 Ω (Note 1, 2)		88		nS		
Turn-On Rise Time	t _R			134		nS		
Turn-Off Delay Time	t _{D(OFF)}			190		nS		
Turn-Off Fall Time	t _F			120		nS		
Total Gate Charge	Q_{G}			38.6		nC		
Gate-Source Charge	Q _{GS}	V_{GS} =10V, V_{DS} =50V, I_{D} =1.3A		11		nC		
Gate-Drain Charge	Q_{GD}	(Note 1, 2)		10.5		nC		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS								
Drain-Source Diode Forward Voltage	V_{SD}	V _{GS} = 0V, I _S = 13 A			1.4	V		
Maximum Continuous Drain-Source Diode	I _S				40	_		
Forward Current					13	Α		
Maximum Pulsed Drain-Source Diode	1				52	^		
Forward Current	I _{SM}				52	Α		

Notes: 1. Pulse Test : Pulse width≤300µs, Duty cycle≤2%

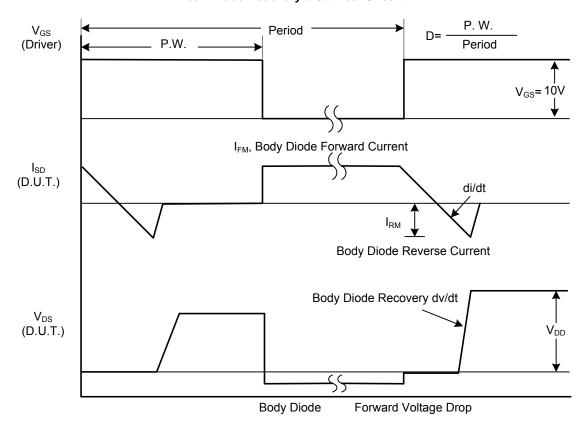
2. Essentially independent of operating ambient temperature



■ TEST CIRCUITS AND WAVEFORMS

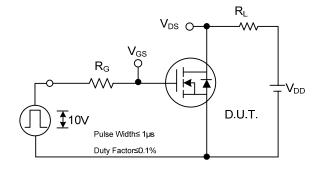


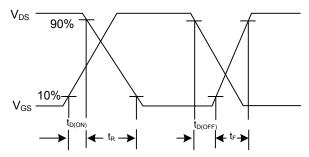
Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

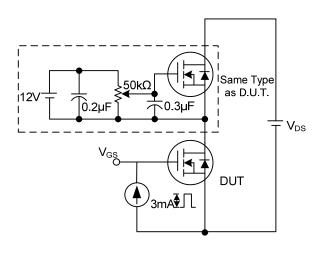
■ TEST CIRCUITS AND WAVEFORMS (Cont.)

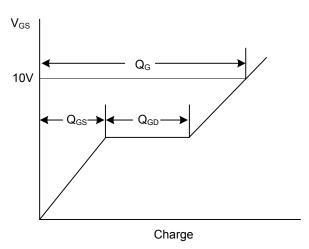




Switching Test Circuit

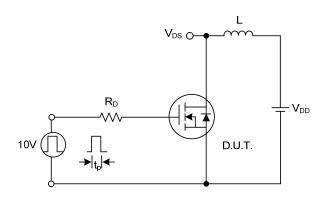
Switching Waveforms

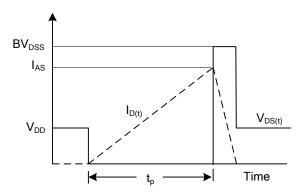




Gate Charge Test Circuit

Gate Charge Waveform





Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

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