



4N65K-MK

Preliminary

Power MOSFET

4A, 650V N-CHANNEL POWER MOSFET

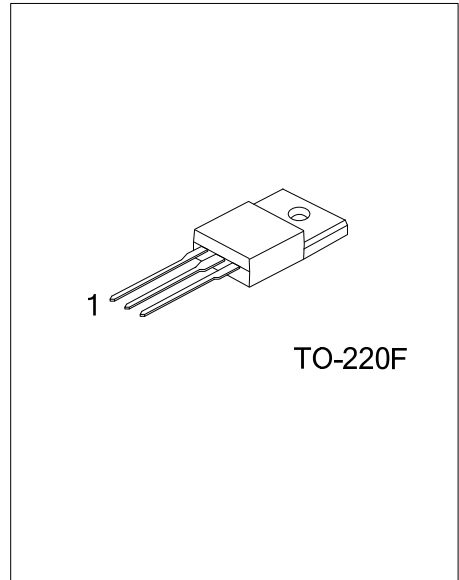
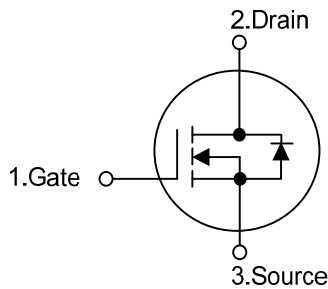
DESCRIPTION

The UTC **4N65K-MK** is a high voltage power MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristic. This power MOSFET is usually used in high speed switching applications including power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} < 3.1\Omega @ V_{GS} = 10V$
- * Fast Switching Capability
- * Avalanche Energy Specified
- * Improved dv/dt Capability, High Ruggedness

SYMBOL



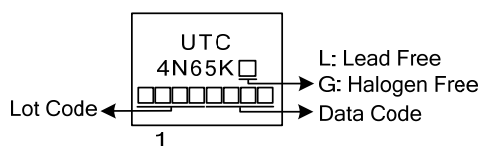
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4N65KL-TF3-T	4N65KG-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>4N65KL-TF3-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) T: Tube (2) TF3: TO-220F (3) L: Lead Free, G: Halogen Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Avalanche Current (Note2)		I_{AR}	4.4	A
Drain Current	Continuous	I_D	4.0	A
	Pulsed (Note2)	I_{DM}	16	A
Avalanche Energy	Single Pulsed (Note3)	E_{AS}	50	mJ
	Repetitive (Note2)	E_{AR}	10.6	mJ
Power Dissipation		P_D	36	W
Derate above 25°C			0.288	W/ $^\circ\text{C}$
Peak Diode Recovery dv/dt (Note4)		dv/dt	4.5	V/ns
Junction Temperature		T_J	+150	$^\circ\text{C}$
Operating Temperature		T_{OPR}	-55 ~ +150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature

3. $L=6.25\text{mH}$, $I_{AS}=4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 4.4\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.57	$^\circ\text{C}/\text{W}$

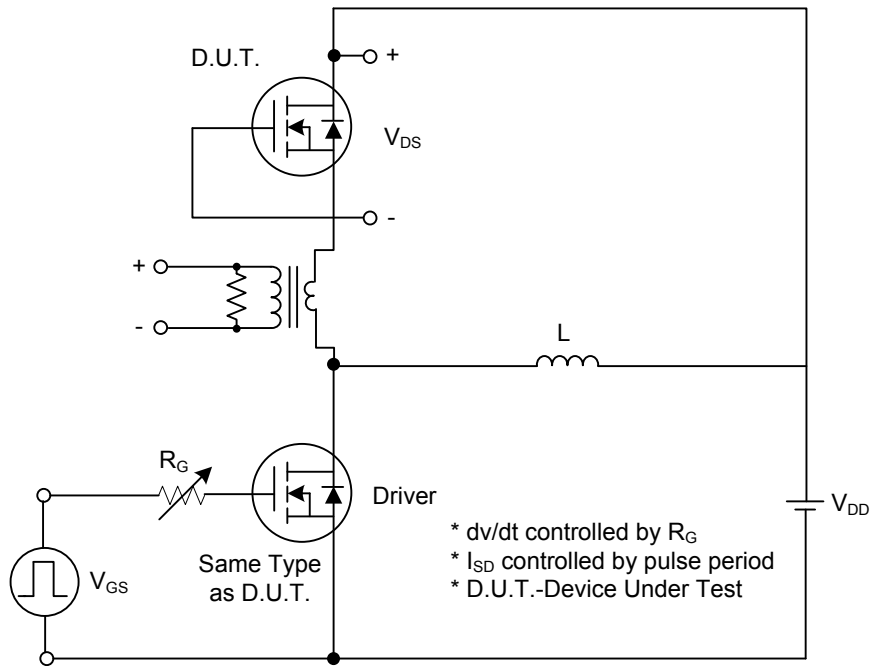
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	650			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
	Reverse				-100	nA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D=250\mu\text{A}$, Referenced to 25°C		0.6		$\text{V}/^\circ\text{C}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 2.2\text{A}$			3.10	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		480	750	pF
Output Capacitance	C_{OSS}			47	90	pF
Reverse Transfer Capacitance	C_{RSS}			5.4	11	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 30\text{V}, I_D = 0.5\text{A},$ $R_G = 25\Omega$ (Note 1, 2)		45		ns
Turn-On Rise Time	t_R			40		ns
Turn-Off Delay Time	$t_{D(OFF)}$			93		ns
Turn-Off Fall Time	t_F			32		ns
Total Gate Charge	Q_G	$V_{DS}= 50\text{V}, I_D= 1.3\text{A},$ $V_{GS}= 10\text{V}$ (Note 1, 2)		17.5	20	nC
Gate-Source Charge	Q_{GS}			5.9		nC
Gate-Drain Charge	Q_{GD}			2.6		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 4.4\text{A}$			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				4.4	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				17.6	A

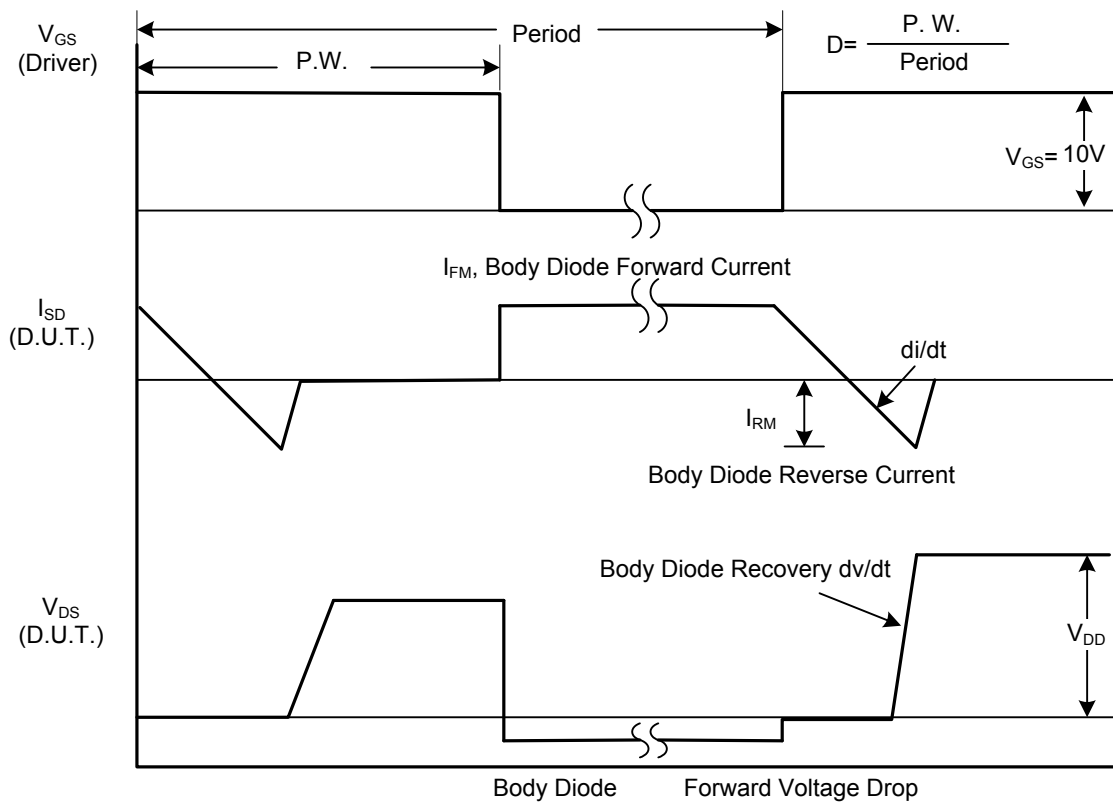
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

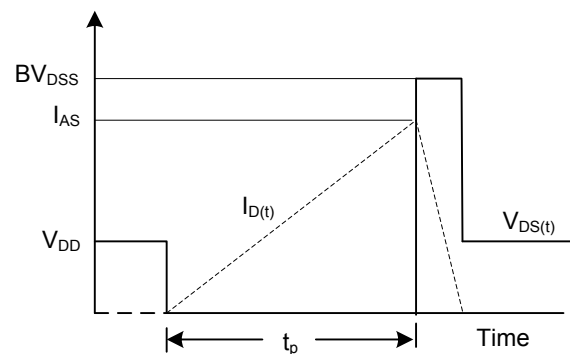
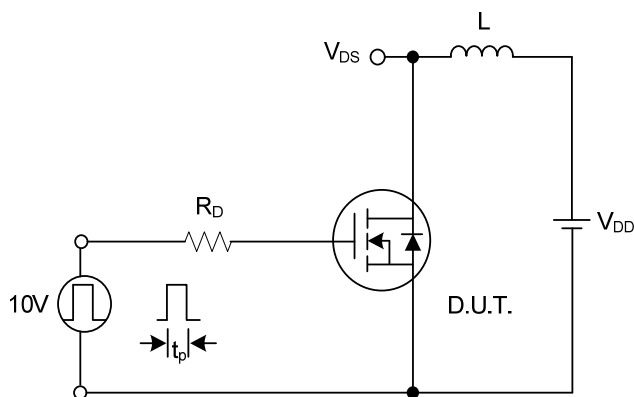
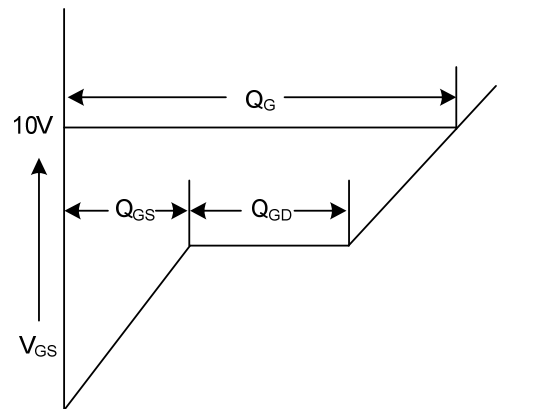
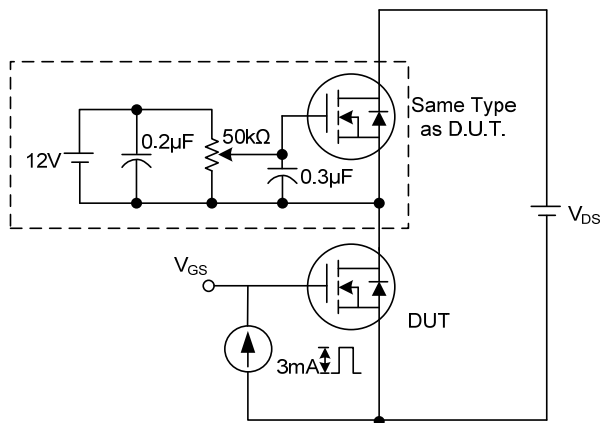
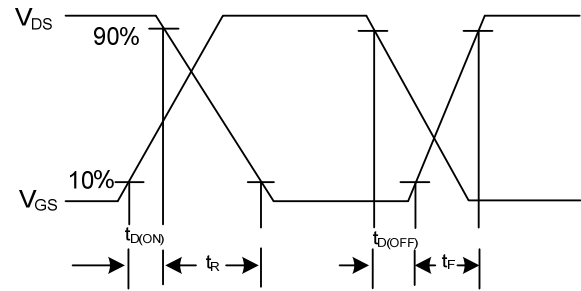
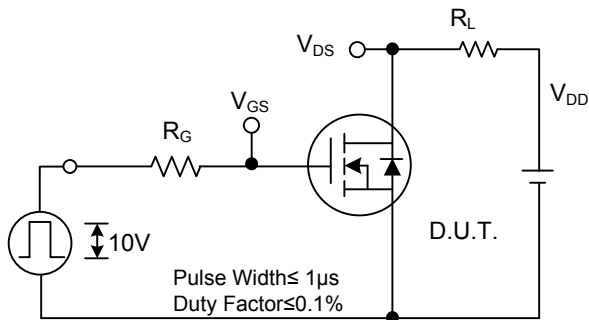


Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)



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