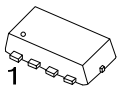
UTT8P03-H

Power MOSFET

-8A, -30V, P-CHANNEL MOSFET



DFN-8(3x2)

■ DESCRIPTION

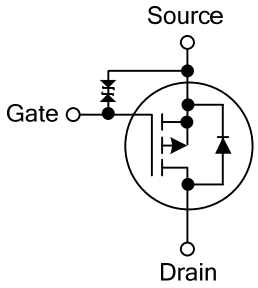
The UTC **UTT8P03-H** is a P-channel MOSFET. it uses UTC's advanced technology to provide the customers with a minimum on state resistance, high switching speed and low gate charge.

The UTC **UTT8P03-H** is suitable for load switching.

■ FEATURES

* $R_{DS(ON)}$ ≤ 26mΩ @ V_{GS}=-10V, I_D=-8A
  $R_{DS(ON)}$ ≤ 34mΩ @ V_{GS}=-4.5V, I_D=-7A
* High switching speed
* Low gate charge

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UTT8P03G-K08-3020-R	DFN-8(3×2)	D	D	D	G	S	D	D	D	Tape Reel

Note: Pin Assignment: D: Drain G: Gate S: Source

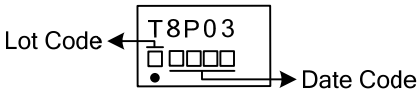
UTT8P03G-K08-3020-R

(1)Packing Type — (1) R: Tape Reel

(2)Package Type — (2) K08-3020: DFN-8(3×2)

(3)Green Package — (3) G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise noted)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	±20	V
Drain Current	Continuous	T_C=25°C	I_D	-8	A
		T_C=70°C		-6	A
	Pulsed (Note 3)		I_{DM}	-60	A
Power Dissipation (Note2)			P_D	3	W
Junction Temperature			T_J	-55~+150	°C
Storage Temperature Range			T_{STG}	-55~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤10s junction-to-ambient thermal resistance.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	90	°C/W
Junction to Case	θ_{JC}	40	°C/W

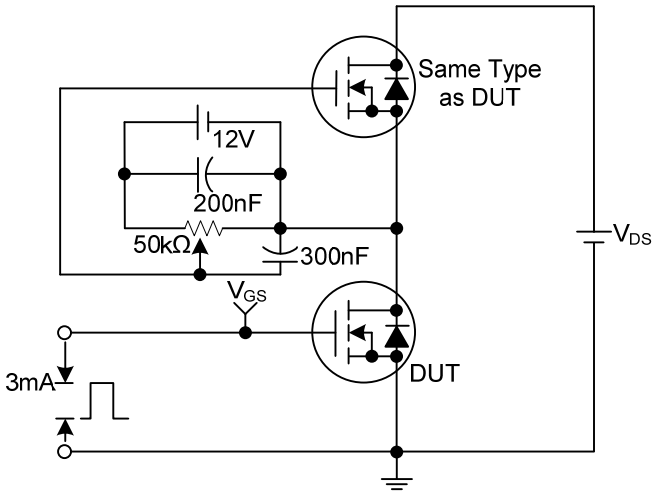
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=-250μA, V_{GS}=0V	-30			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=-30V, V_{GS}=0V			-1	μA
			V_{DS}=-30V, V_{GS}=0V, T_J=55°C			-5	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+10	uA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-10	uA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.8	-1.3	-1.8	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=-10V, I_D=-8A		21	26	mΩ
			V_{GS}=-4.5V, I_D=-7A		27	34	mΩ
On State Drain Current		$I_{D(ON)}$	V_{GS}=-10V, V_{DS}=-5V	-60			A
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=-15V, f=1.0MHz		930		pF
Output Capacitance		C_{OSS}			170		pF
Reverse Transfer Capacitance		C_{RSS}			120		pF
Gate Resistance		R_G	V_{GS}=0V, V_{DS}=0V, f=1MHz		8		Ω
SWITCHING PARAMETERS (Note 2)							
Total Gate Charge		Q_G	V_{GS}=-4.5V, V_{DS}=-15V, I_D=-5A		11	17	nC
Gate to Source Charge		Q_{GS}			3.4		nC
Gate to Drain Charge		Q_{GD}			4.2		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DS}=-1 5V, V_{GS}=-10V, R_{GEN}=6Ω, I_D=-1A		5.8	11	ns
Rise Time		t_R			18.8	36	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			46.9	90	ns
Fall-Time		t_F			12.3	23	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				-8.5	A
Maximum Body-Diode Pulsed Current		I_{Sm}				-17	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=-1A, V_{GS}=0V		-0.74	-1	V

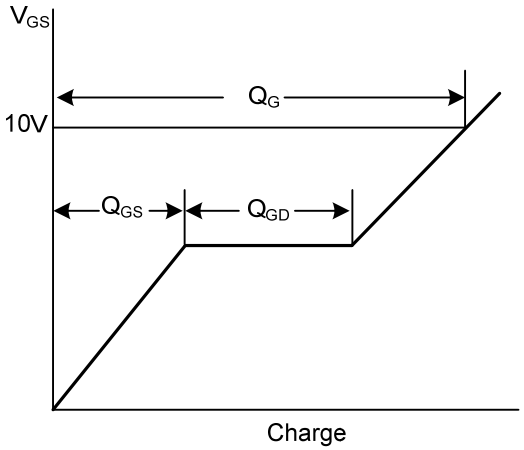
Notes: 1. The value of θ_{JA} is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤10s junction-to-ambient thermal resistance.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C
4. The θ_{JA} is the sum of the thermal impedance from junction to lead θ_{JL} and lead to ambient
5. The static characteristics in Figures 1 to 6 are obtained using <300us pulses, duty cycle 0.5% max
6. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

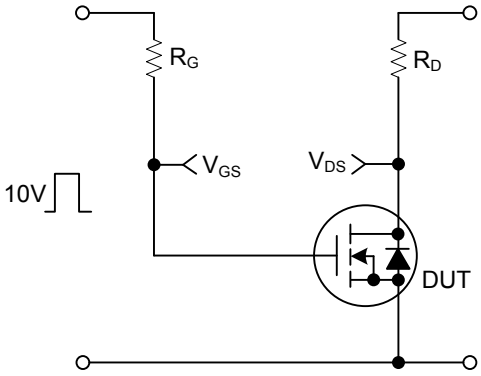
■ TEST CIRCUITS AND WAVEFORMS



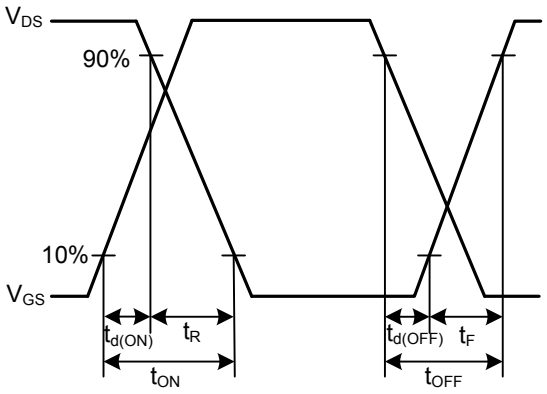
Gate Charge Test Circuit



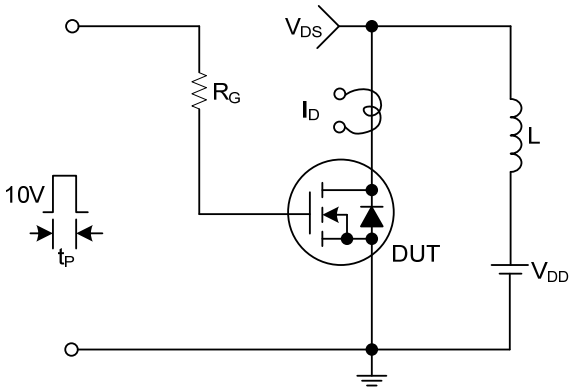
Gate Charge Waveforms



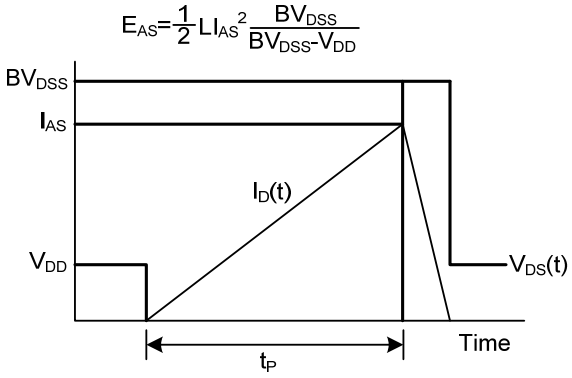
Resistive Switching Test Circuit



Resistive Switching Waveforms

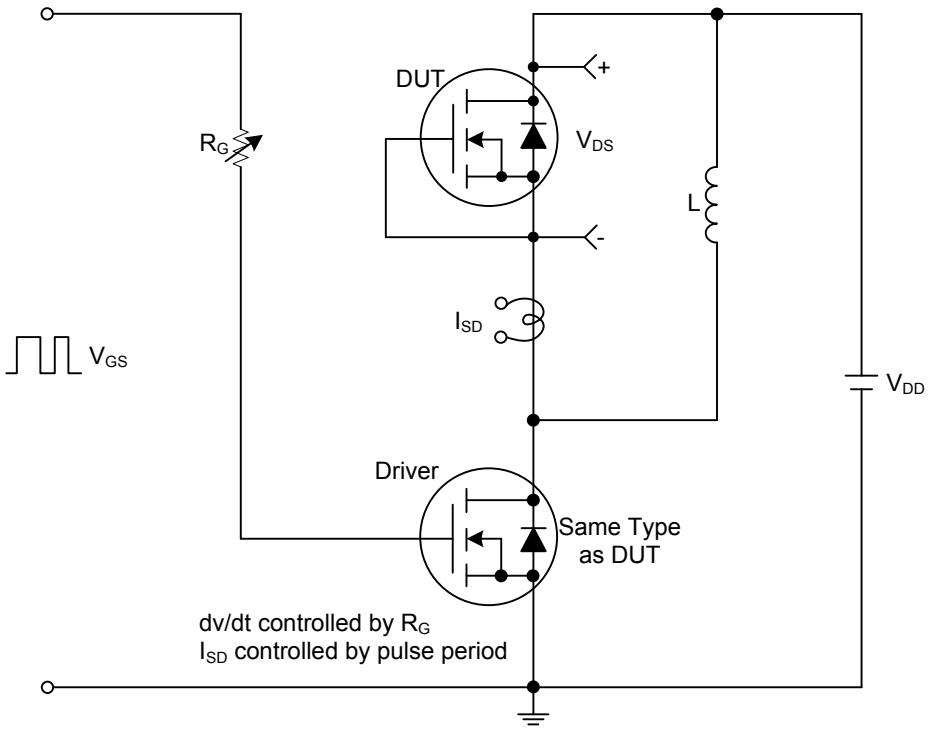


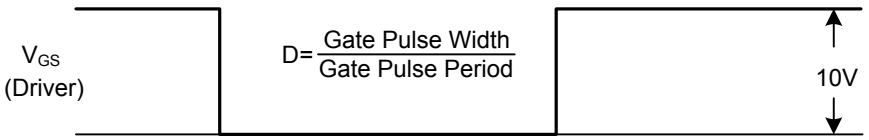
Unclamped Inductive Switching Test Circuit

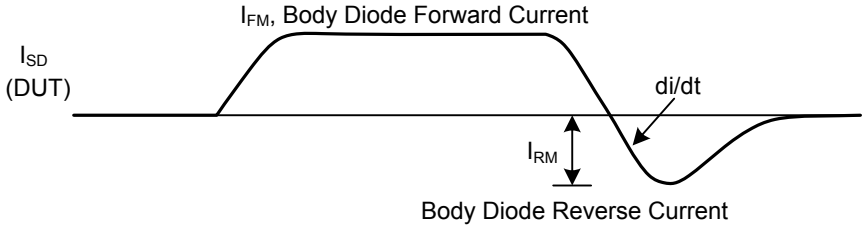


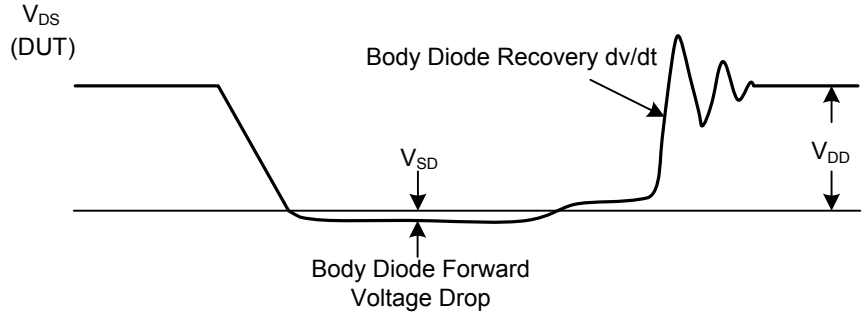
Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)









Peak Diode Recovery dv/dt Test Circuit and Waveforms

■ TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics (Note 5)

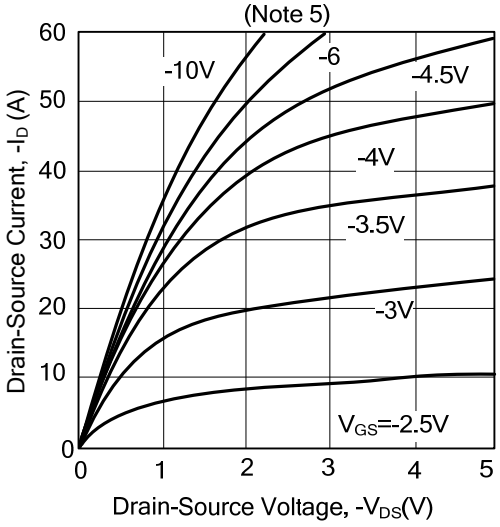


Figure 2. Transfer Characteristics (Note 5)

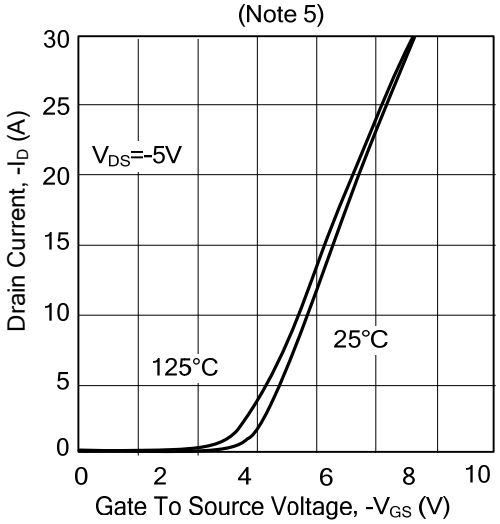


Figure 3. On-Resistance vs. Drain Current and Gate Voltage (Note 5)

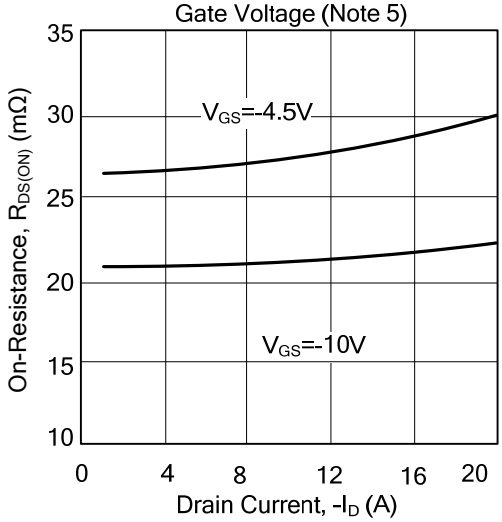


Figure 4. On-Resistance vs. Junction Temperature (Note 5)

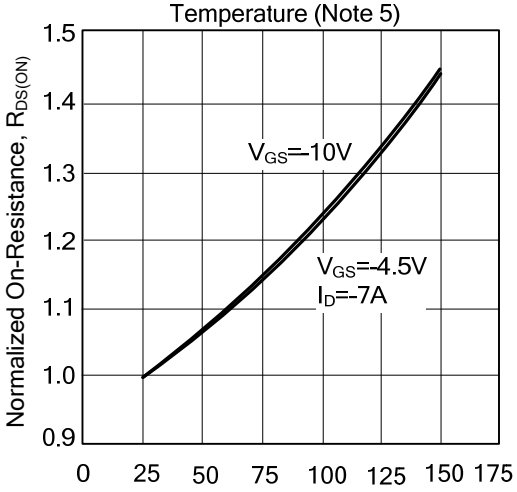


Figure 5. On-Resistance vs. Gate-Source Voltage (Note 5)

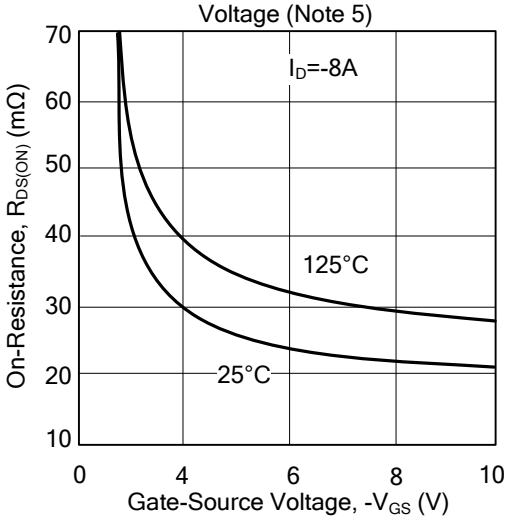
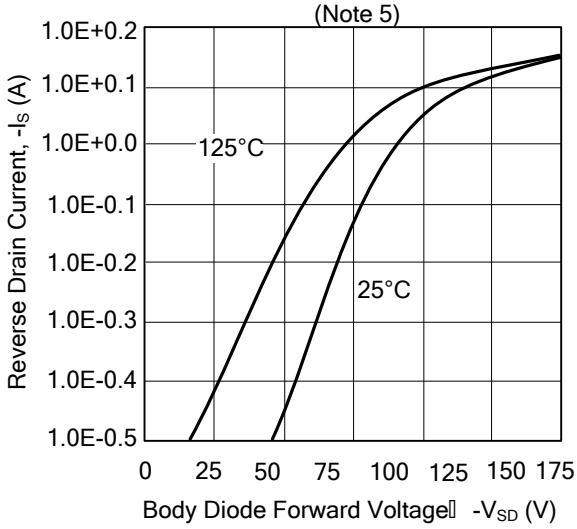


Figure 6. Body-Diode Characteristics (Note 5)



■ TYPICAL CHARACTERISTICS (Cont.)

Figure 7. Capacitance Characteristics (Note 5)

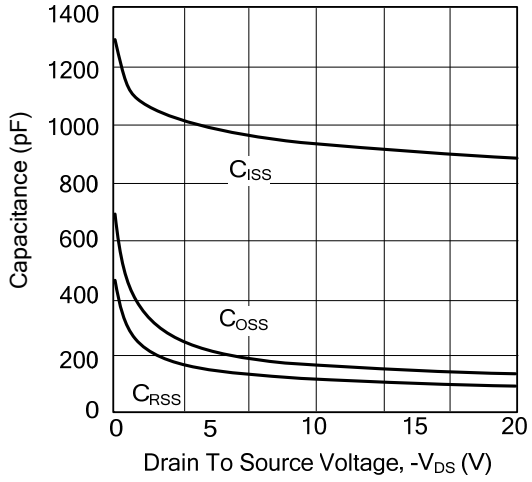


Figure 8. Maximum Forward Biased Safe Operation Area (Note 6)

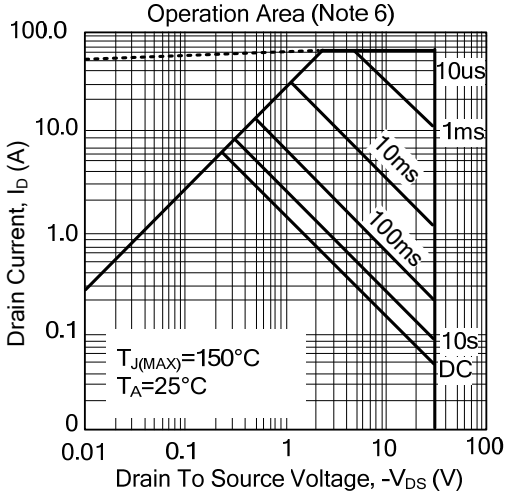


Figure 9. Single Pulse Power Rating Junction-to-Ambient (Note 6)

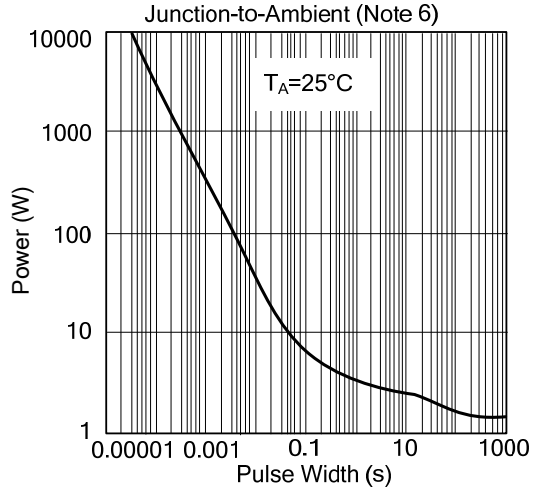


Figure 10: Normalized Maximum Transient Thermal Impedance (Note 6)

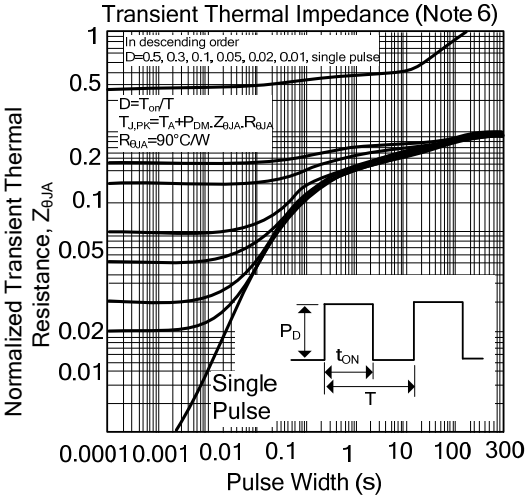


Figure 11: Normalized Maximum Transient Thermal Impedance (Note 6)