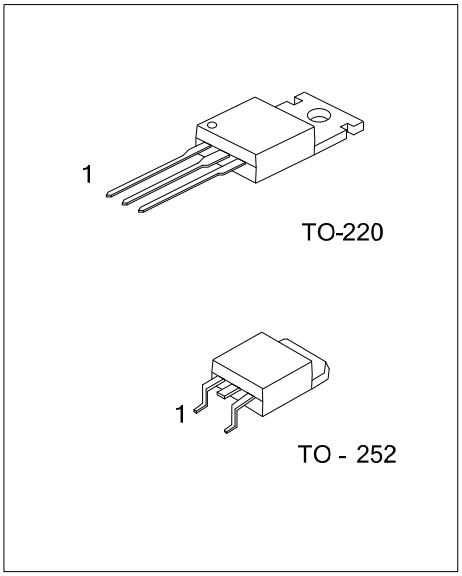
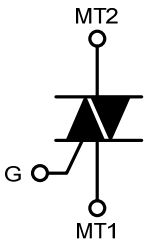
TRIAC



■ DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

■ SYMBOL



■ ORDERING INFORMATION

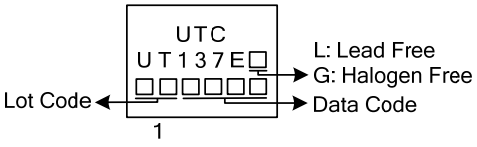
Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
UT137EL-x-TA3-T	UT137EG-x-TA3-T	TO-220	MT1	MT2	GATE	Tube
UT137EL-x-TN3-R	UT137EG-x-TN3-R	TO-252	MT1	MT2	GATE	Tape Reel

UT137EL-x-TA3-T

(1)Packing Type
(2)Package Type
(3)Peak Voltage
(4)Lead Free

(1) T: Tube, R: Tape Reel
(2) TA3: TO-220, TN3: TO-252
(3) 5: 500V, 6: 600V, 8: 800V
(4) L: Lead Free, G: Halogen Free

■ MARKING



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages	UT137E-5	V_{DRM}	500 (Note 2)	V
	UT137E-6		600 (Note 2)	V
	UT137E-8		800	V
RMS on-state current full sine wave; T_{mb} ≤102°C		$I_{T(RMS)}$	8	A
Non-repetitive peak on-state current (Full sine wave; T_J = 25°C prior to surge)	t = 20ms	I_{TSM}	65	A
	t = 16.7 ms		71	
I^2t for fusing	t = 10 ms	I^2t	21	A^2s
Repetitive rate of rise of on-state current after triggering I_{TM}=12A; I_G=0.2A; d_{IG} /dt=0.2A/μs	T2+ G+	dI_T /dt	50	A/μs
	T2+ G-		50	A/μs
	T2- G-		50	A/μs
	T2- G+		10	A/μs
Peak gate voltage		V_{GM}	5	V
Peak gate current		I_{GM}	2	A
Peak gate power		P_{GM}	5	W
Average gate power (over any 20 ms period)		$P_{G(AV)}$	0.5	W
Junction Temperature		T_J	125	°C
Storage Temperature		T_{STG}	-40 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6A/μs.

■ THERMAL RESISTANCES

PARAMETER			SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance Junction to Ambient	In Free Air	TO-220	$θ_{JA}$		60		°C/W
		TO-252			15		
Thermal resistance Junction to mounting base	Full cycle	TO-220	$θ_{JC}$			2.0	°C/W
		TO-252				2.6	
	Half cycle	TO-220				2.4	°C/W
		TO-252				3.0	

■ STATIC CHARACTERISTICS (T_J=25°C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gate trigger current	I_{GT}	V_D = 12 V; I_T = 0.1 A	T2+G+		2.5	10	mA
			T2+G-		4.0	10	mA
			T2-G-		5.0	10	mA
			T2-G+		11	25	mA
Latching current	I_L	V_D = 12 V; I_{GT} = 0.1 A	T2+G+		3.0	25	mA
			T2+G-		14	35	mA
			T2-G-		3.0	25	mA
			T2-G+		4.0	35	mA
Holding current	I_H	V_D = 12 V; I_{GT} = 0.1 A			2.5	20	mA
On-state voltage	V_T	I_T = 10 A			1.3	1.65	V
Gate trigger voltage	V_{GT}	V_D = 12 V; I_T = 0.1 A			0.7	1.5	V
		V_D = 400V ; I_T = 0.1 A; T_J =125°C		0.25	0.4		V
Off-state leakage current	I_D	V_D = $V_{DRM(max)}$; T_J= 125°C			0.1	0.5	mA

■ DYNAMIC CHARACTERISTICS (T_J=25°C, unless otherwise stated)

parameter	symbol	conditions	min	typ	max	unit
Critical rate of rise of Off-state voltage	d_{VD} /dt	V_{DM} = 67% V_{DRMMAX} ; T_J=125°C; Exponential waveform; gate open		50		V/μs

		circuit				
Gate controlled turn-on time	t_{GT}	I_{TM} = 12A; V_D= V_{DRMMAX} ; I_G=0.1A; d_{IG}/dt=5A/μs		2		μs

■ TYPICAL CHARACTERISTICS

Figure 1. Maximum On -State Dissipation. P_{tot} vs RMS On-State Current, $I_{T(RMS)}$, Where α=conduction Angle

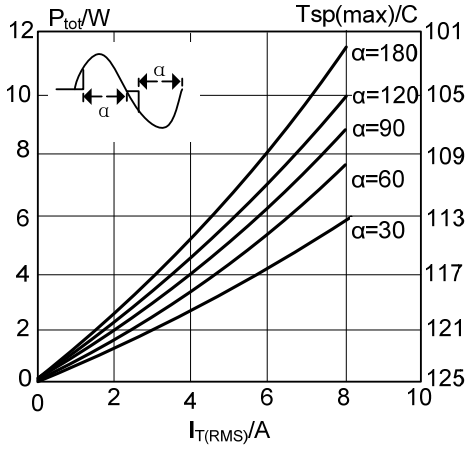


Figure 2. Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM}, vs Pulse Width t_p, for Sinusoidal Currents, $t_p \leqq 20ms$

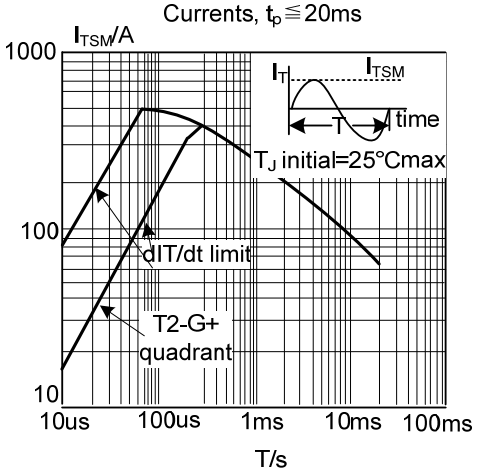


Figure 3 .Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM}, vs Number of Cycles, for Sinusoidal Currents, f=50Hz

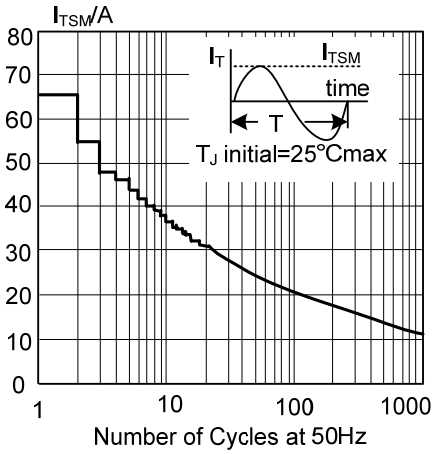


Figure 4. Maximum Permissible RMS Current $I_{T(RMS)}$ vs Mounting Base Temperature T_{mb}

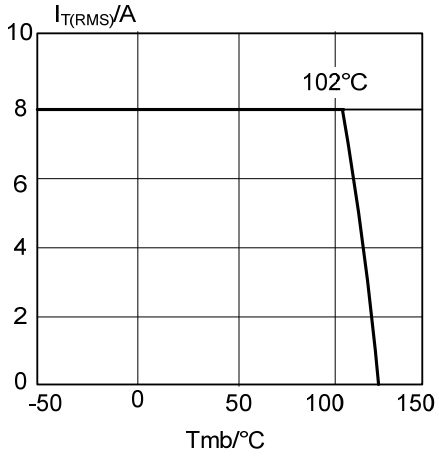


Figure 5. Maximum Permissible Repetitive RMS On-State Current $I_{T(RMS)}$, vs Surge Duration, for Sinusoidal Currents,f =50Hz, $T_{mb} \leqq 102°C$

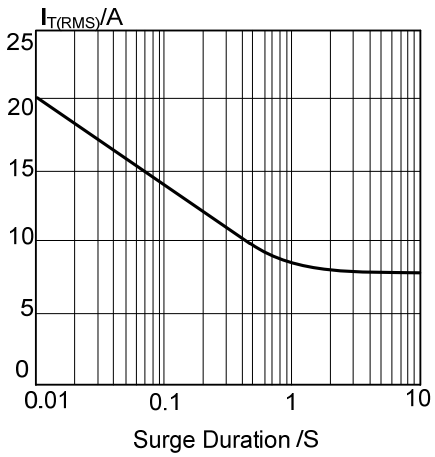
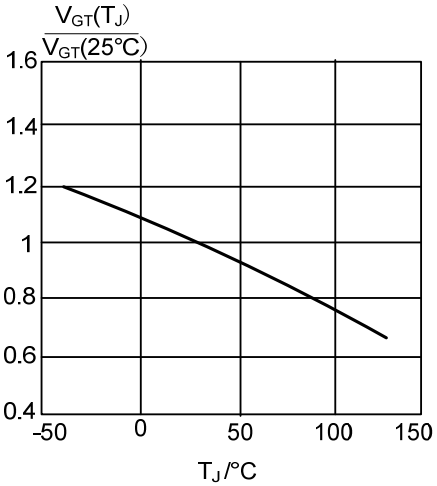


Figure 6. Normalised Gate Trigger Voltage $V_{GT}(T_J)/V_{GT}(25°C)$, vs Junction Temperature T_J



■ TYPICAL CHARACTERISTICS(Cont.)

Figure 7. Normalised Gate Trigger Current $I_{GT}(T_J)/I_{GT}(25°C)$, vs Junction Temperature T_J

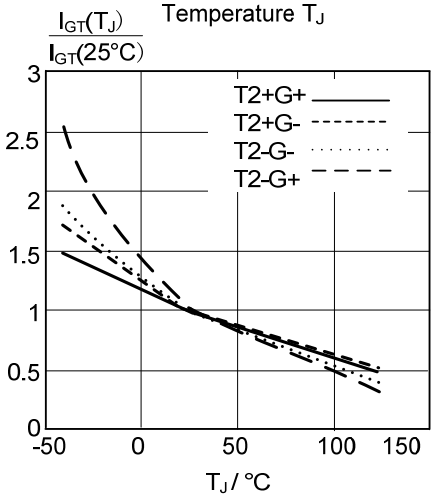


Figure 8. Normalised Latching Current $I_L(T_J)/I_L(25°C)$, vs Junction Temperature T_J

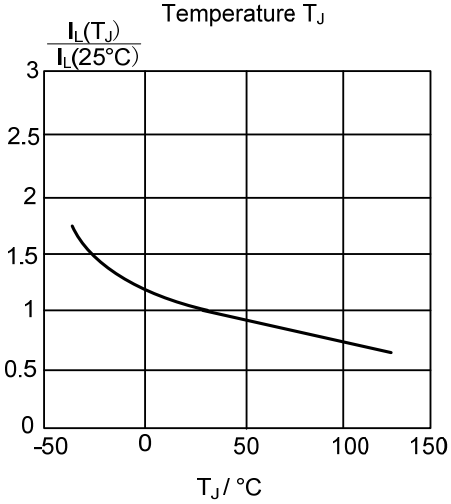


Figure 9. Normalised Holding Current $I_H(T_J)/I_H(25°C)$, vs Junction Temperature T_J

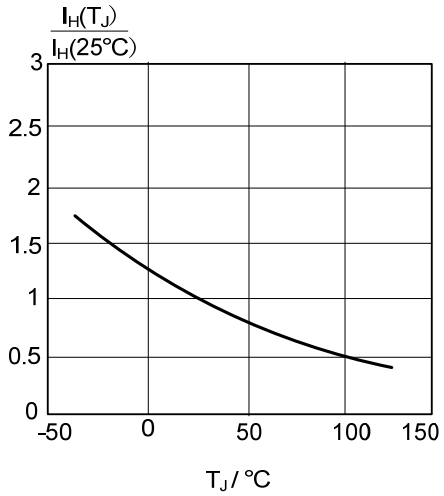


Figure 10. Typical and Maximum On-state Characteristic

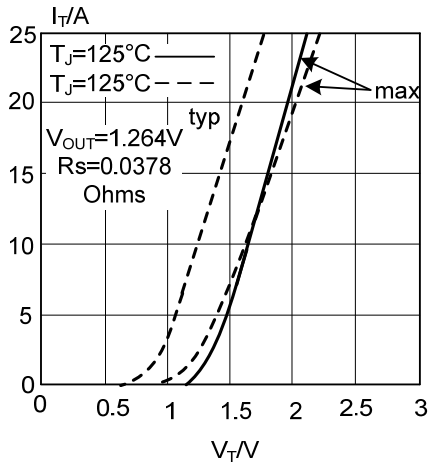


Figure 11. Transient Thermal Impedance $Z_{th\ j\text{-}mb}$, vs Pulse Width t_p

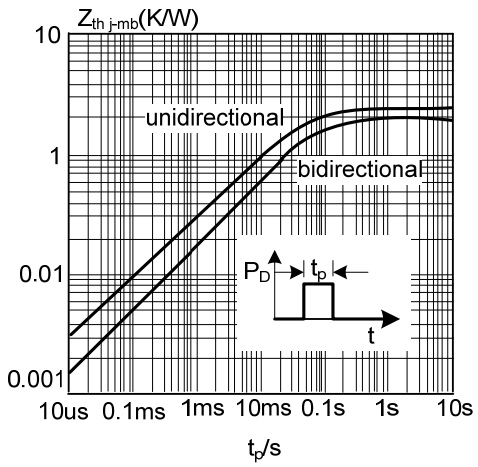


Figure 12. Typical Critical Rate of Rise of Off-State Voltage, dV_D/dt Versus Junction temperature T_J