

UNISONIC TECHNOLOGIES CO., LTD

UOT406 Preliminary TRIAC

FOUR-QUADRANT TRIAC, ENHANCED NOISE IMMUNITY

■ DESCRIPTION

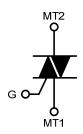
The UTC **UOT406** is a Four-quadrant triac, it uses UTC's advanced technology to provide customers with direct interfacing to low power gate drive circuits and sensitive gate, etc.

The UTC **UOT406** is suitable for Low power AC fan speed controllers, Low power motor control and Home appliances, etc.

■ FEATURES

- * $V_{DRM} \le 600V$, $I_{GT} \le 3mA$, $I_{GT} \le 5mA$ (T2-G+) $I_{TSM} \le 12.5A$ (t=20ms), $I_{TSM} \le 13.8A$ (t=16.7ms), $I_{T(RMS)} \le 1A$
- * Direct interfacing to low power gate drive circuits
- * Sensitive gate

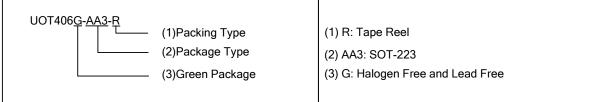
■ SYMBOL



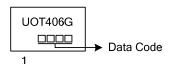
■ ORDERING INFORMATION

Ordering Number	Package	Pin Assignment			Dooking	
		1	2	3	Packing	
UOT406G-x-AA3-R	SOT-223	MT1	MT2	G	Tape Reel	

Note: Pin Assignment: MT1: MT1 MT2: MT2 G: Gate



■ MARKING



1 SOT-223

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■ ABSOLUTE MAXIMUM RATINGS

PARAME	TER		SYMBOL	YMBOL RATINGS		
Repetitive Peak Off-State Voltage			V_{DRM}	600	٧	
Repetitive Peak Reverse Voltage			V _{RRM} 600		٧	
RMS On-State Current	full sine wave, T _{sp} ≤	103°C	I _{T(RMS)}	1	Α	
Non-Repetitive Peak On-State Current	full sine wave, T _J ≤25°C prior to	t=20ms		12.5	Α	
	surge	t=16.7ms	I _{TSM}	13.8	Α	
I ² t for Fusing	t _p =10ms		l ² t	1.28	A^2s	
Rate of Rise of On-State Current	I_{TM} =1A, I_{G} =20mA, dI_{G} /dt=0.2A/ μ s	T2+G+	dl _⊤ /dt	50	A/µs	
		T2+G-		50	A/µs	
		T2-G-		50	A/µs	
		T2-G+		10	A/µs	
Peak Gate Current			I_{GM}	1	Α	
Peak Gate Power			P_GM	2	W	
Average Gate Power	Over any 20ms period		$P_{G(AV)}$	0.1	W	
Storage Temperature			T_{STG}	-40 ~ +150	°C	
Junction Temperature		T_J	125	°C		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL RESISTANCES

PARA	PARAMETER		MIN	TYP	MAX	UNIT
Junction to Case		θ_{JC}			15	K/W
Junction to Ambient	For minimum footprint	θ_{JA}		156		K/W
	For pad area			70		K/W

■ **ELECTRICAL CHARACTERISTICS** (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gate Trigger Current	I _{GT}		T2+G+			3	mA
		V _D =12V, I _T =0.1A	T2+G-			3	mA
			T2-G-			3	mA
			T2-G+			5	mA
Cata Trigger Voltage	V_{GT}	V _D =12V, I _T =0.1A				1.3	V
Gate Trigger Voltage		$V_D = V_{DRM}, I_T = 0.1A, T_J = 125^{\circ}C$		0.2			V
Holding Current	lΗ	V _D =12V, I _G =0.1A			7	mA	
Latching Current	IL	V _D =12V, I _G =0.1A	T2+G+			7	mA
			T2+G-			20	mA
			T2-G-			7	mA
			T2-G+			7	mA
On-State Voltage	V_{T}	I _T =1A			1.3	1.6	V
Off-State Current	I _D	V _D =V _{DRM(max)} , T _J =125°C			0.5	mA	
Rate of Rise of Off-State Voltage	dV _D /dt	V _{DM} =0.67V _{DRM} (max), T _J =110°C, exponential waveform, gate open circuit		10			V/µs
Rate of Change of Commutating Voltage	dV _{com} /dt	V _{DM} =400V, T _J =110°C, I _{TM} =1A, dI _{com} /dt= 0.44A/ms		0.5			V/µs

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