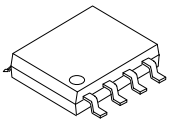
M4334 **CMOS IC**

STEREO AUDIO D/A CONVERTER 24BITS,96KHZ SAMPLING



SOP-8

■ DESCRIPTION

The UTC **M4334** is a complete low cost stereo audio digital to analog converter(DAC), its contains interpolation, 1-bit D/A conversion and analog output filtering. The **M4334** is based on a 4th order $\Delta-\Sigma$ modulation, where the modulator output controls the reference voltage input to an ultra-liner analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

The **M4334** also contains digital de-emphasis function, operates from a single +5V power supply, for best performance, decoupling capacitors should be located as close to the device package as possible with the smallest capacitor closest, the **M4334** requires minimal support circuitry.

The **M4334** is ideal for DVD players, set-top boxes, SVCD players and A/V receivers.

■ FEATURES

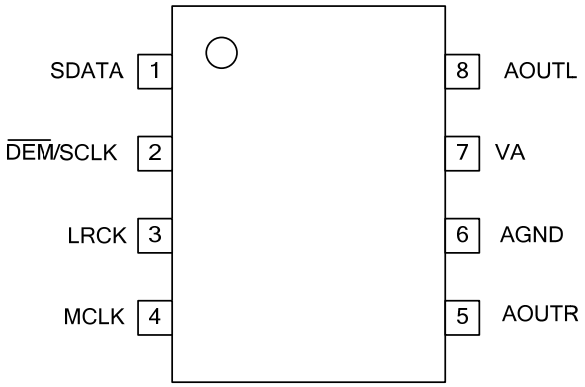
* Complete stereo DAC: Includes Output Analog Filter and DAC
* Dynamic Range: 96dB
* THD+N: -88dB
* Multiple Sampling Frequencies: 16kHz to 96kHz
* Low Clock Jitter Sensitivity
* Single Power Supply: 5V
* Filtered Line Level Outputs
* On-Chip Digital De-emphasis
* Normal or I2S Data Input Formats
* 24Bits Conversion

■ ORDERING INFORMATION

Ordering Number	Package	Packing
M4334G-S08-R	SOP-8	Tape Reel

M4334G-S08-T (1)Packing Type (2)Package Type (3)Halogen Free	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free

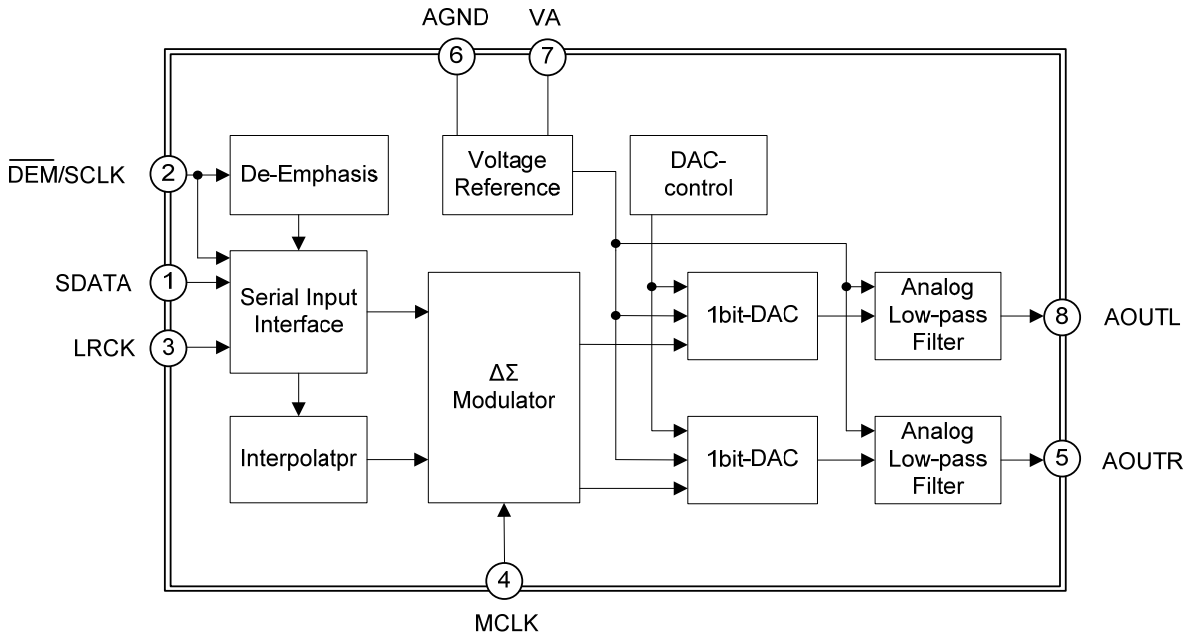
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN NO	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	SDATA	I	Serial audio data input: two's complement MSB-first serial data is input on this pin. The data is clocked into the **M4334** via internal or external SCLK, and the channel is determined by LRCK.
2	DEM/SCLK	I	De-emphasis control and clock input for audio data: used for de-emphasis filter control or external serial clock input.
3	LRCK	I	Sample rata clock input: determines which channel is currently being input on the audio serial data input pin.
4	MCLK	I	System clock input: frequency must be 256x, 384x, or 512x the input sample rate in BRM and either 128x or 192x the input sample rate in HRM.
5	AOUTR	O	Right-channel analog output
6	AGND	I	Ground pin
7	VA	I	Power supply pin for the internal control circuits
8	AOUTL	O	Left-channel analog output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
DC Power Supply	V_A	-0.3~6	V
Digital Input Voltage	V_{IND}	-0.3~ VA +0.4	V
Input Current, Any Pin Except Supplies	I_{IN}	±10	mA
Ambient Operating Temperature	T_A	-55 ~ +125	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS(Note1)

PARAMETER	SYMBOL	RANGE	UNIT
DC Power Supply	V_A	4.75 ~ 5.5	V

Note: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.
2. The VOUT tracks the VREF with additional voltage offset and load regulation.

■ ELECTRICAL CHARACTERISTICS

All specifications at 25°C,VA=+5V, full-scale output sine wave,997Hz; MCLK=12.288MHz; Fs for =48kHz, SCLK=3.072MHz, measurement bandwidth 10Hz to 20kHz, unless otherwise specified; f_S for HRM=96kHz, SCLK=6.144MHz, measurement bandwidth 10Hz to 40kHz, unless otherwise specified. RL=10KΩ, CL=10pF.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER AND THERMAL						
Power supply current	I_A	Normal operation		15	19	mA
		Power-down state		40		uA
Power Dissipation	P_D	Normal operation		75	104	mW
		Power-down state		0.2		
Package Thermal Resistance	θ_{JA}			110		°C /W
Power Supply Rejection Ratio	PSRR	f=1kHz		79		dB
DC ACCURACY						
Inter Channel Gain Mismatch				0.1	0.4	dB
Gain Error				±5		%
Gain Drift				100		ppm/°C
ANALOG OUTPUT						
Full Scale Output Voltage			3.25	3.5	3.75	Vpp
Quiescent Voltage	V_Q			2.2		VDC
Max AC-Load Resistance	R_L			3		KΩ
Max Load Capacitance	C_L			100		pF
DIGITAL INPUT/OUTPUT						
High-Level Input Voltage	V_{IH}		2.0			V
Low-Level Input Voltage	V_{IL}				0.8	V
Input Leakage Current	$I_{I(Leak)}$				±10	μA
Input Capacitance	C_{IN}			8		pF

■ ELECTRICAL CHARACTERISTICS (Cont.)

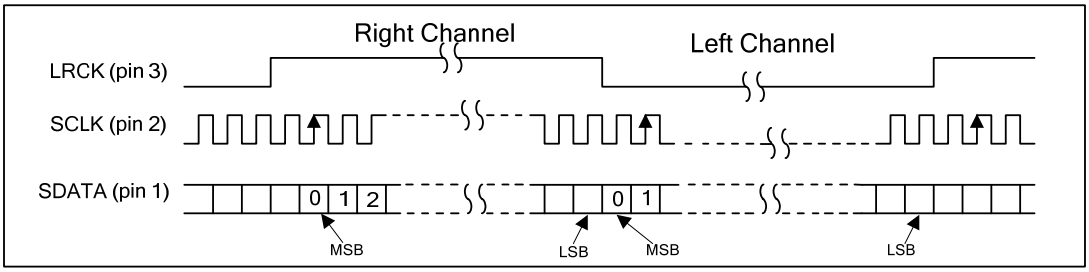
PARAMETER	SYMBOL	TEST CONDITIONS	Base-Rate Mode			High-Rate Mode			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Ambient Operating Temperature	T_{OPR}		-40		85	-40		85	°C
Dynamic Range		16-bit , un-weighted	83	91			88		dB
		16-bit , a-weighted	86	94		86	94		
		18 to 24-bit, un-weighted	85	93			90		
		18 to 24-bit , a-weighted	88	96		88	96		
Total Harmonic Distortion +Noise	THD+N	16-bit, 0dB		-86	-70		-86	-80	dB
		16-bit, -20dB		-71	-63		-68	-60	
		16-bit, -60dB		-31	-23		-28	-20	
		18 to 24-bit, 0dB		-88	-82		-88	-82	
		18 to 24-bit, -20dB		-73	-65		-70	-62	
		18 to 24-bit, -60dB		-33	-25		-30	-22	

■ SWITCHING CHARCTERISTICS

(T_A=-40 to 85°C;VA=4.75V~5.5V; Input: Logic 0=0V, Logic 1=V_A, C_L=20pF)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Sample Rate	f_S		2		100	kHz
MCLK Pulse Width High		MCLK/LRCK=512	10		1000	ns
MCLK Pulse Width Low		MCLK/LRCK=512	10		1000	ns
MCLK Pulse Width High		MCLK/LRCK=384 or 192	21		1000	ns
MCLK Pulse Width Low		MCLK/LRCK=384 or 192	21		1000	ns
MCLK Pulse Width High		MCLK/LRCK=256 or 128	31		1000	ns
MCLK Pulse Width Low		MCLK/LRCK=256 or 128	31		1000	ns
EXTERNAL SCLK MODE						
LRCK Duty Cycle			40	50	60	%
SCLK Pulse Width High	t_{SCLKH}		20			ns
SCLK Pulse Width Low	t_{SCLKL}		20			ns
SCLK Period	t_{SCLKW}	MCLK/LRCK=512,256 or 384	$\frac{1}{(128)\,Fs}$			ns
		MCLK/LRCK=128 or 192	$\frac{1}{(64)\,Fs}$			ns
SCLK rising to LRCK edge delay	t_{SLRD}		20			ns
SCLK rising to LRCK edge setup time	t_{SLRS}		20			ns
SDATA valid to SCLK rising setup time	t_{SDLRS}		20			ns
SCLK rising to SDATA hold time	t_{SDH}		20			ns
INTERNAL SCLK MODE						
LRCK duty cycle				50		%
SCLK Period	t_{SCLKW}		$\frac{1}{SCLK}$			ns
SCLK rising to LRCK edge	t_{SCLKR}			$\frac{tsclkw}{2}$		µs
SDATA valid to SCLK rising setup time	t_{SDLRS}		$\frac{1}{(512)\,Fs}+10$			ns
SCLK rising to SDATA hold time	t_{SDH}	MCLK/LRCK=128 , 256 or 512	$\frac{1}{(512)\,Fs}+15$			ns
SCLK rising to SDATA hold time	t_{SDH}	MCLK/LRCK=192 or 384	$\frac{1}{(384)\,Fs}+15$			ns

■ TIMING DIAGRAMS



Inernal SCLK Mode	External SCLK Mode
I^2S, 16-Bit data and internal SCLK=32fs if MCLK/LRCK=128, 256 or 512	I^2S, up to 24-Bit data Data valid on rising edge of SCLK
I^2S, up to 24-Bit data and internal SCLK=48fs if MCLK/LRCK=192 or 384	

Figure 1. I^2S Data Input Timing

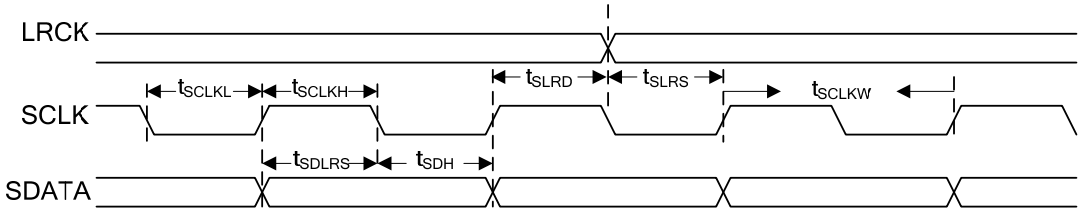


Figure 2. Audio Data Input Timing

■ TYPICAL APPLICATION CIRCUIT

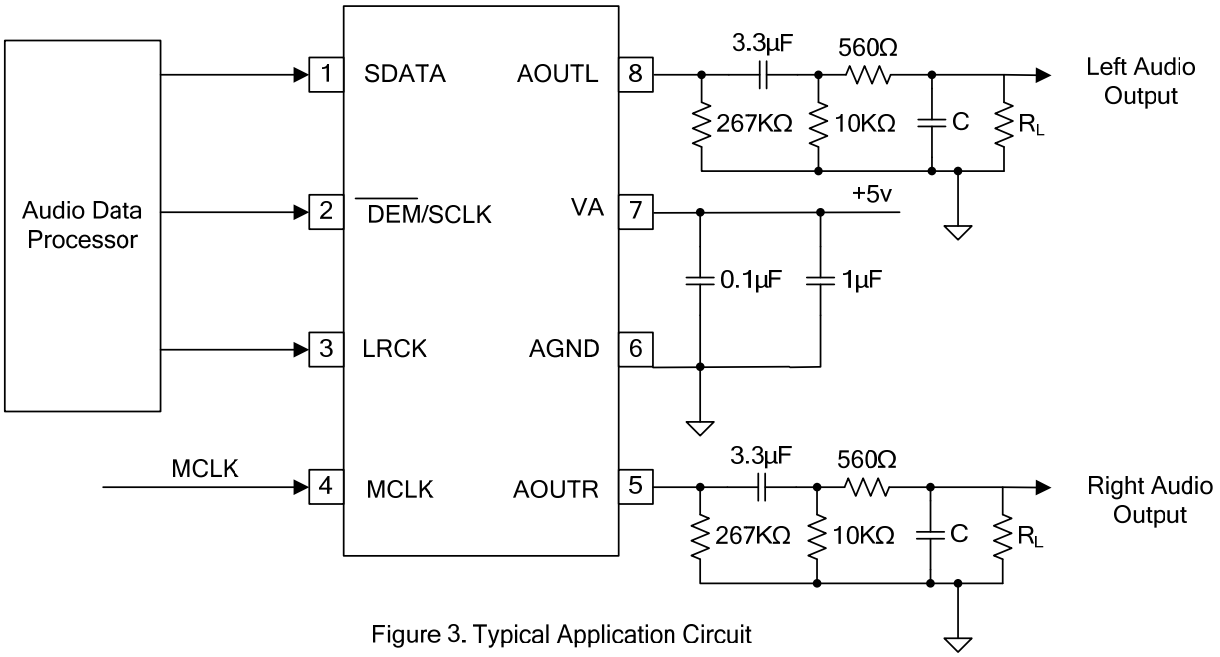


Figure 3. Typical Application Circuit

■ APPLICATION CONSIDERATION

The **M4334** is a complete low cost stereo digital-to-analog output system contains digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis and analog low pass filter. The **M4334** used the ΔΣ modulation techniques is to avoid the limitations of resistive laser trimmed DAC architectures by using an inherently linear 1-bit DAC.

The **M4334** supports two modes of operation. The devices operate in Base Rate Mode (BRM) when MCLK/LRCK is 256, 384 or 512 and in High Rate Mode (HRM) when MCLK/LRCK is 128 or 192. HRM allows input sample rates up to 100 kHz.

The **M4334** also has the de-emphasis function, the de-emphasis filter is active when the DEM/SCLK pin is low for 5 consecutive falling edges of LRCK, but this function is available only in the internal SCLK mode.

When the **M4334** is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. After a sh- ort delay of approximately 1000 sample periods, each output begins to ramp towards its quiescent voltage, VQ. App- roximately 10,000 sample cycles later, the outputs reach VQ and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to VQ, effectively blocking the quiescent DC voltage.

To prevent transients at power-down, the device must first enter its power-down state. This is accomplished by rem- oving MCLK or LRCK. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. A soft-start current sink is substituted in place of AOUTL and AOUTR which allows the DC-blo- cking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off, and the system is ready for the next power-on.

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning off the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance.

■ SYSTEM CLOCK

The **M4334** accepts data at standard audio sample rates including 48, 44.1 and 32 kHz in BRM and 96, 88.2 and 64 kHz in HRM. The LRCK chooses the channel and delineation of data, and the SCLK clocks audio data into the input data buffer.

MCLK

MCLK must be either 256x, 384x or 512x the desired input sample rate in BRM and either 128x or 192x the desired input sample rate in HRM. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period. Internal dividers are set to generate the proper clocks. The MCLK, LRCK and SCLK must be synchronous. Table 1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK(kHz)	MCLK(MHz)				
	HRM		BRM		
	128x	192x	256x	384x	512x
32	4.0960	6.1440	8.1920	12.2880	16.3840
44.1	5.6448	8.4672	11.2896	16.9344	22.5792
48	6.1440	9.2160	12.2880	18.4320	24.5760
64	8.1920	12.2880			
88.2	11.2896	16.9344			
96	12.2880	18.4320			

Table 1. Common Clock Frequencies

SCLK

The SCLK controls the shifting of data into the input data buffers. The **M4334** supports both internal and external SCLK generation modes.

Internal SCLK Mode

In the Internal SCLK Mode, the SCLK is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, or 64 depending upon data format. Operation in this mode is identical to operation w- ith an external SCLK synchronized with LRCK. This mode allows access to the digital de-emphasis function.

While the Internal SCLK Mode is provided to allow access to the de-emphasis filter, the Internal SCLK Mode also eliminates possible clock interference from an external SCLK.

External SCLK Mode

The **M4334** will enter the external SCLK mode when 16 low to high transitions are detected on the DEM/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal SCLK Mode and de-emphasis filter cannot be accessed. The **M4334** will switch to Internal SCLK Mode if no low to high transitions are detected on the DEM/SCLK pin for 2 consecutive frames of LRCK.