

UTC UNISONIC TECHNOLOGIES CO., LTD

22N65 **Power MOSFET**

22A, 650V N-CHANNEL POWER MOSFET

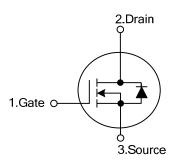
DESCRIPTION

As the SMPS MOSFET, the UTC 22N65 uses UTC's advanced technology to provide excellent R_{DS(ON)}, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

FEATURES

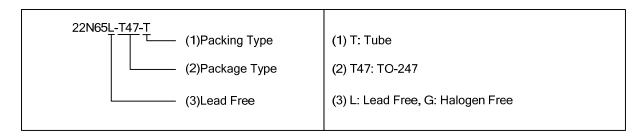
- * $R_{DS(ON)} = 0.35\Omega$
- * Ultra low gate charge (Typical 150 nC)
- * Low reverse transfer capacitance (C_{RSS} = typical 36 pF)
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

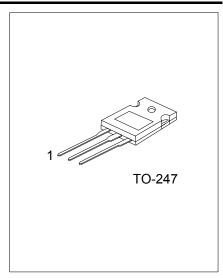
SYMBOL



ORDERING INFORMATION

Ordering Number		Dookogo	Pin Assignment			Dooking	
Lead Free	Halogen Free	Package	1	2	3	Packing	
22N65L-T47-T	22N65G-T47-T	TO-247	G	D	S	Tube	





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■ ABSOLUTE MAXIMUM RATINGS (T_C =25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		V _{DSS}	650	V	
Gate-Source Voltage		V_{GSS}	±30	V	
Avalanche Current		I _{AR}	22	Α	
Continuous Drain Current		I_{D}	22	Α	
Pulsed Drain Current (Note 1)		I _{DM}	88	Α	
Avalanche Energy	Single Pulsed	E _{AS}	380	mJ	
	Repetitive	E _{AR}	37	mJ	
Peak Diode Recovery dv/dt (Note 2)		dv/dt	18	V/ns	
Power Dissipation		P_D	370	W	
Junction Temperature		TJ	150	°C	
Operating Temperature		T _{OPR}	-55 ~ + 150	°C	
Storage Temperature		T _{STG}	-55 ~ + 150	°C	

Note: 1. Repetitive rating; pulse width limited by max. junction temperature.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT	
Junction to Ambient	θ_{JA}	40	°C /W	
Junction to Case	θ _{JC}	0.30	°C /W	

ELECTRICAL CHARACTERISTICS(T_J=25°C, L=1.5mH,R_G=25Ω,I_{AS} =22A,Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
OFF CHARACTERISTICS								
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650			V		
Drain-Source Leakage Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V			50	μA		
Gate- Source Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±30V			±100	nA		
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_{J}$	I _D =1mA, Referenced to 25°C		0.30		V/°C		
ON CHARACTERISTICS								
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu A$	2.0		4.0	٧		
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =13A (Note 2)		0.3	0.35	Ω		
DYNAMIC PARAMETERS								
Input Capacitance	C_{ISS}			3200		pF		
Output Capacitance	Coss	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		350		pF		
Reverse Transfer Capacitance	C_{RSS}			36		pF		
SWITCHING PARAMETERS								
Turn-ON Delay Time	$t_{D(ON)}$			100		ns		
Turn-ON Rise Time	t_R	V_{DD} =300V, I_{D} =22A, R_{G} =6.2 Ω ,		250		ns		
Turn-OFF Delay Time	t _{D(OFF)}	V _{GS} =10V (Note 2)		650		ns		
Turn-OFF Fall-Time	t _F]		550		ns		
Total Gate Charge	Q_G	\\ -400\\ \\ -10\\ -22A			150	nC		
Gate Source Charge	Q_GS	V _{DS} =480V, V _{GS} =10V, I _D =22A			45	nC		
Gate Drain Charge	Q_GD	(Note 2)			76	nC		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS								
Drain-Source Diode Forward Voltage	V_{SD}	V _{GS} =0V, I _S =22A			1.5	V		
Continuous Source Current (Body Diode)	Is	(Note 1)			22	Α		
Pulsed Source Current (Body Diode)	I _{SM}				88	Α		
Reverse Recovery Time	t _{RR}	I _S =22A,		590	890	ns		
Reverse Recovery Charge	Q_{RR}	di/dt=100A/µs (Note 2)		7.2	11	μC		

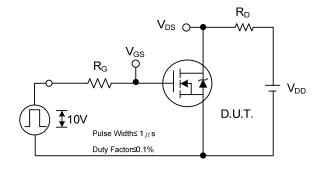
Note: 1. Repetitive rating; pulse width limited by max. junction temperature.

^{2.} $I_{SD} \le 22A$, di/dt ≤ 540 A/ μ s, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 150$ °C.

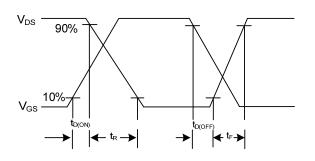
^{3.} Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

^{2.} Pulse Width ≤ 300 s, Duty Cycle ≤ 2%.

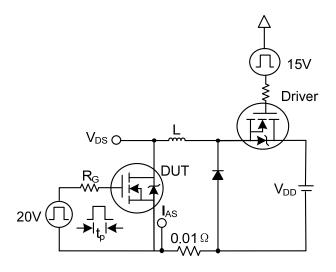
■ TEST CIRCUITS



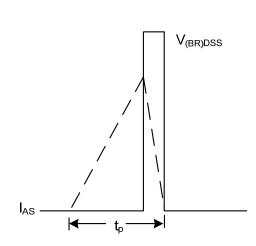
Switching Test Circuit



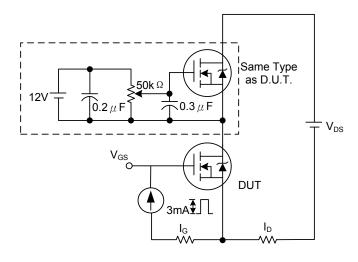
Switching Waveforms



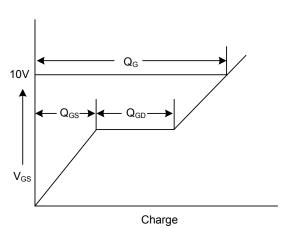
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



Gate Charge Test Circuit



Gate Charge Waveform

■ TEST CIRCUITS(Cont.)

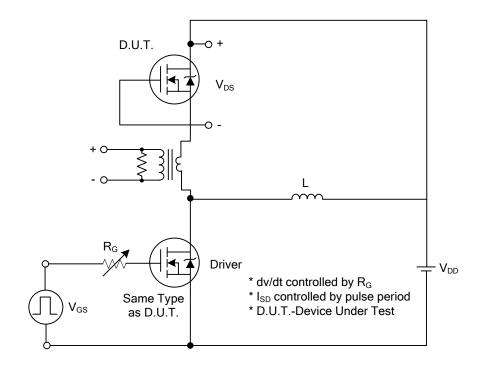
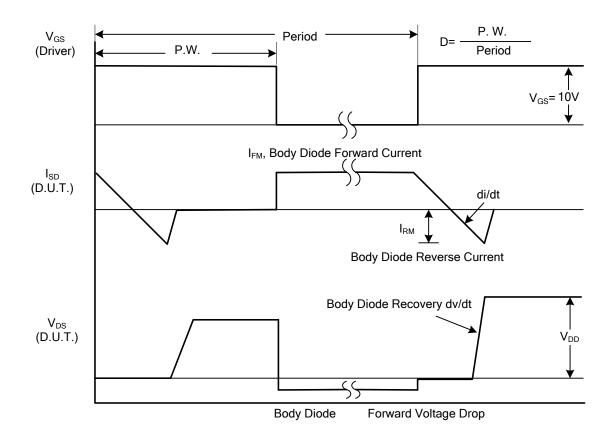
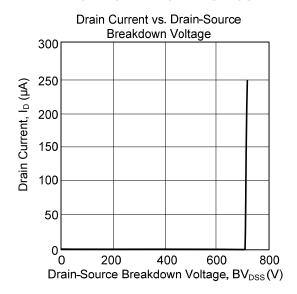
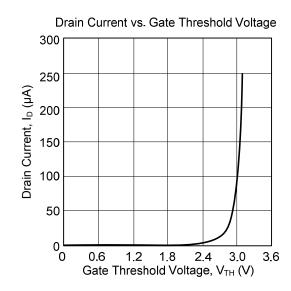


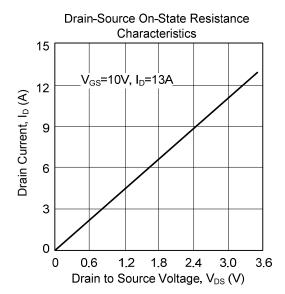
Fig. 1A Peak Diode Recovery dv/dt Test Circuit

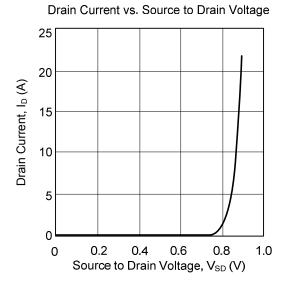


■ TYPICAL CHARACTERISTICS









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