



1N50Z

Power MOSFET

1.3A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

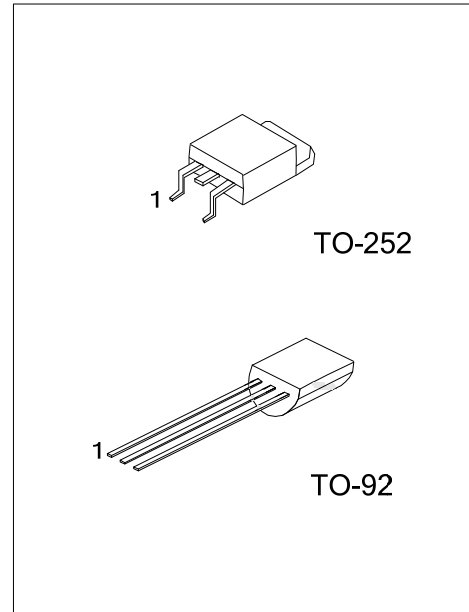
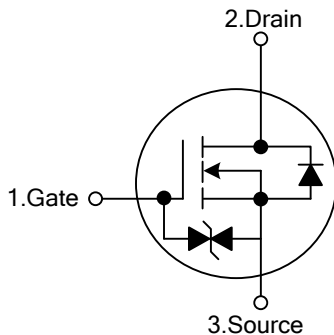
The UTC **1N50Z** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **1N50Z** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

FEATURES

- * $R_{DS(ON)} < 6.0\Omega @ V_{GS}=10V$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



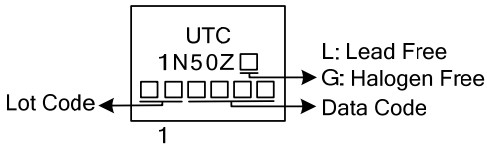
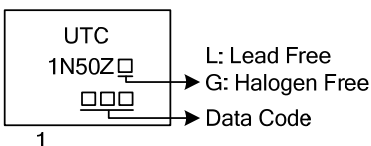
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
1N50ZL-T92-B	1N50ZG-T92-B	TO-92	G	D	S	Tape Box
1N50ZL-T92-K	1N50ZG-T92-K	TO-92	G	D	S	Bulk
1N50ZL-TN3-R	1N50ZG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>1N50ZL-T92-B</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Lead Free</p>	<p>(1) B: Tape Box, K: Bulk, R: Tape Reel</p> <p>(2) T92: TO-92, TN3: TO-252</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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MARKING

TO-252	TO-92
 <p>Diagram of TO-252 marking: A rectangular box contains the text "UTC" and "1N50Z" followed by a small square. Below this is a row of five small squares. An arrow labeled "Lot Code" points to the first square. An arrow labeled "Data Code" points to the last square. Below the row of squares is the number "1". To the right of the box, the text "L: Lead Free" and "G: Halogen Free" is shown with an arrow pointing to the right.</p>	 <p>Diagram of TO-92 marking: A rectangular box contains the text "UTC" and "1N50Z" followed by a small square. Below this is a row of two small squares. An arrow labeled "Data Code" points to the last square. Below the row of squares is the number "1". To the right of the box, the text "L: Lead Free" and "G: Halogen Free" is shown with an arrow pointing to the right.</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous ($T_C=25^\circ\text{C}$)	I_D	1.3 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	5 (Note 2)	A
Avalanche Current (Note 3)		I_{AR}	1.3	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	113	mJ
	Repetitive (Note 5)	E_{AR}	2.6	mJ
Power Dissipation	TO-92	P_D	40	W
	TO-252		45	
Derate above 25°C	TO-92		0.32	W/ $^\circ\text{C}$
	TO-252		0.36	
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Drain current limited by maximum junction temperature
3. Repetitive Rating: Pulse width limited by maximum junction temperature
4. $I_{SD} \leq 1.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-92	θ_{JA}	160	$^\circ\text{C}/\text{W}$
	TO-252		110	
Junction to Case	TO-92	θ_{JC}	80	$^\circ\text{C}/\text{W}$
	TO-252		4.53	

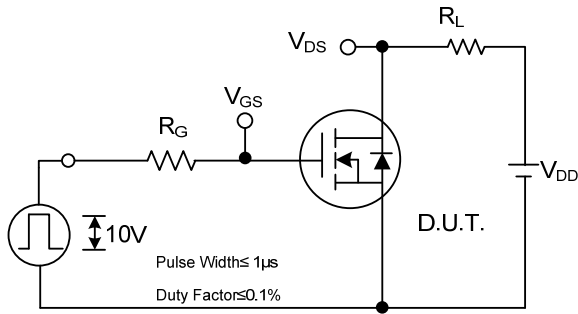
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}			+5	μA
	Reverse				-5	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=0.5\text{A}$		4.6	6.0	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		220	290	pF
Output Capacitance	C_{OSS}			30	35	pF
Reverse Transfer Capacitance	C_{RSS}			11	13	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $I_D=1.3\text{A}$ (Note 1, 2)		12.5	16	nC
Gate to Source Charge	Q_{GS}			3.2		nC
Gate to Drain Charge	Q_{GD}			2.7		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		20	35	ns
Rise Time	t_R			40	50	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			70	90	ns
Fall-Time	t_F			48	60	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				1.3	A
Maximum Body-Diode Pulsed Current	I_{SM}				5	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=1.3\text{A}$, $V_{GS}=0\text{V}$			1.15	V
Body Diode Reverse Recovery Time	t_{rr}	$I_S=1.5\text{A}$, $V_{GS}=0\text{V}$,		130		ns
Body Diode Reverse Recovery Charge	Q_{RR}	$di_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		0.32		μC

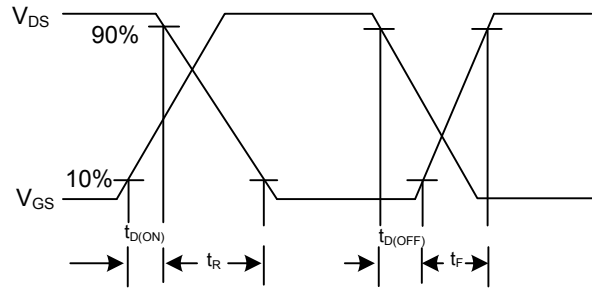
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

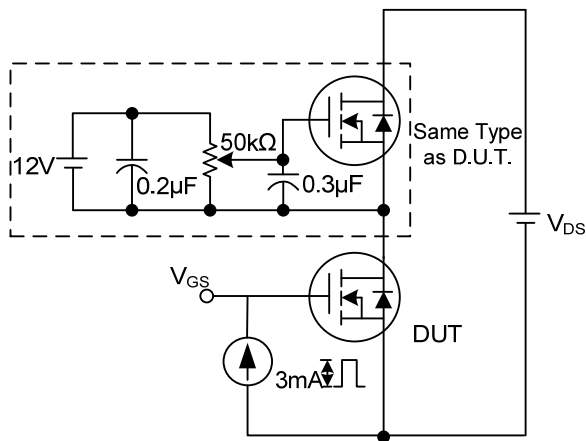
TEST CIRCUITS AND WAVEFORMS



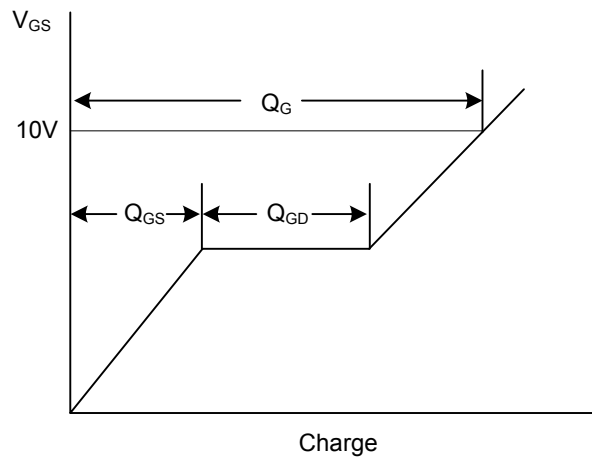
Switching Test Circuit



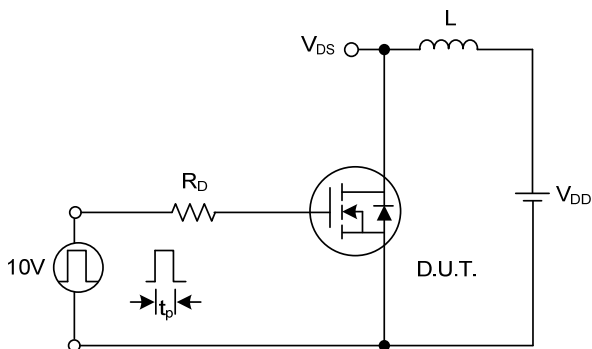
Switching Waveforms



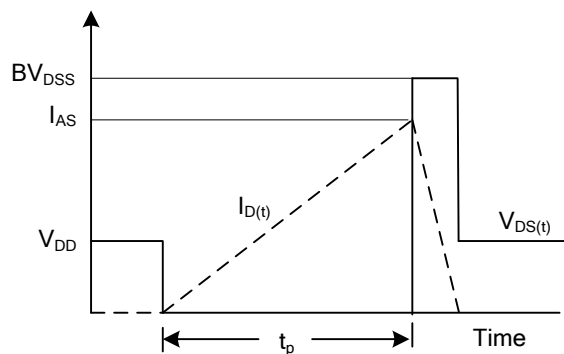
Gate Charge Test Circuit



Gate Charge Waveform

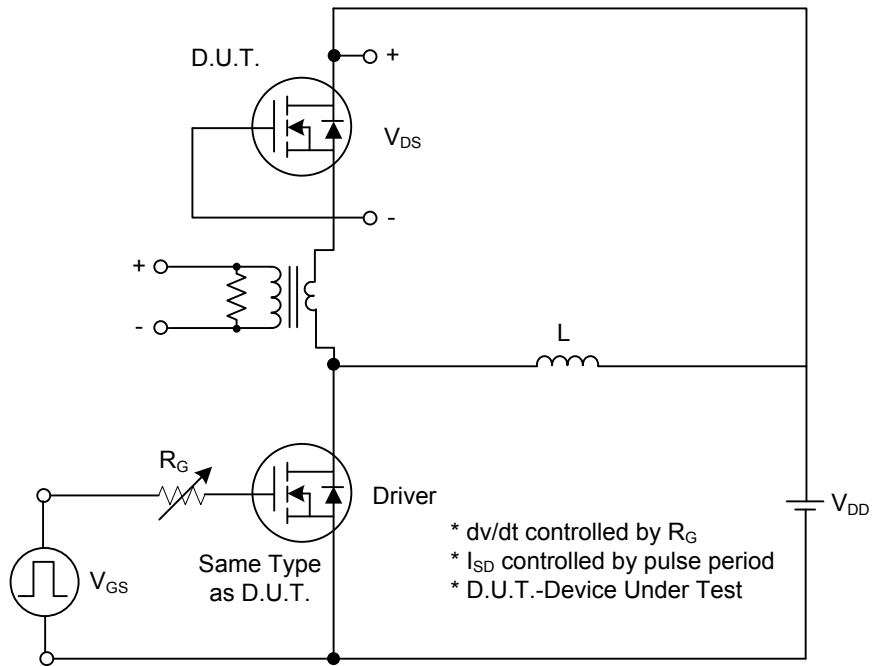


Unclamped Inductive Switching Test Circuit

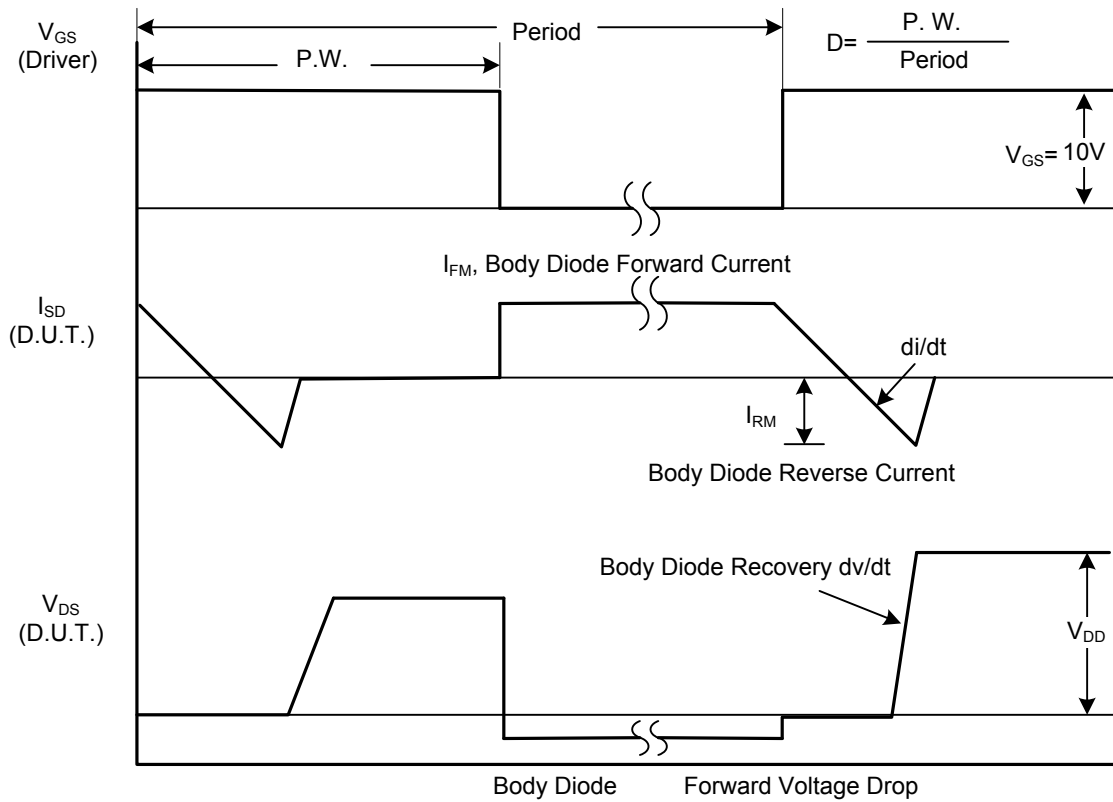


Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)

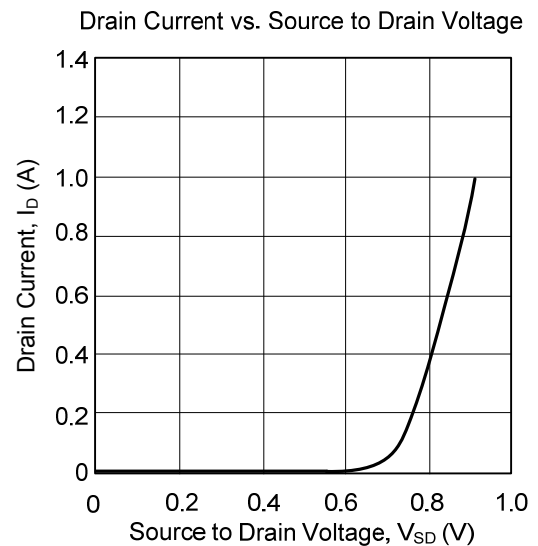
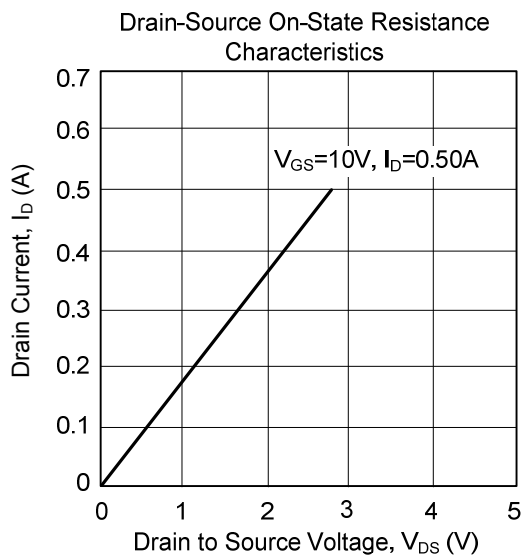
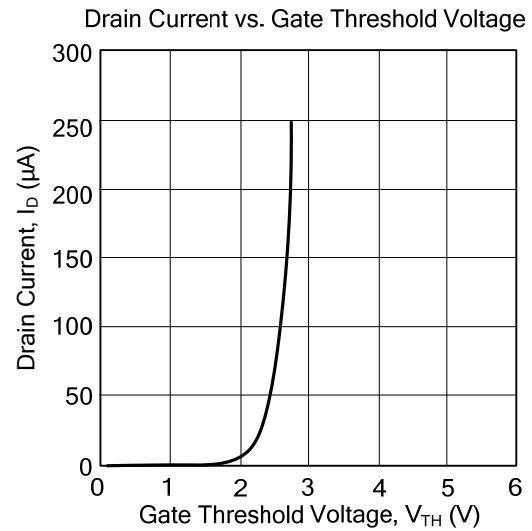
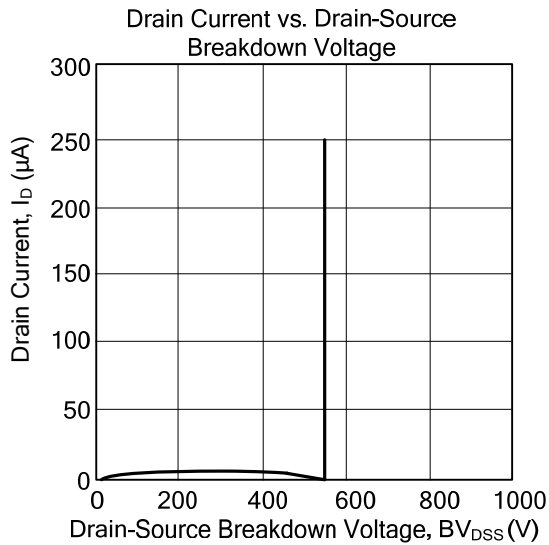


Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

TYPICAL CHARACTERISTICS



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