



UF1404

Preliminary

Power MOSFET

162A, 40V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **UF1404** is a N-channel enhancement power MOSFET using UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$ and high switching speed.

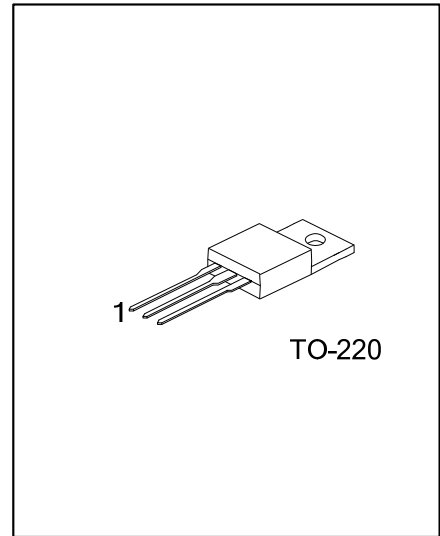
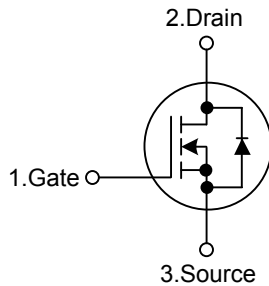
The UTC **UF1404** is suitable for all commercial-industrial applications at power dissipation levels to approximately 50 watts, etc.

FEATURES

* $R_{DS(ON)} = 4m\Omega @ V_{GS}=10V, I_D=95A$

* High Switching Speed

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF1404L-TA3-T	UF1404G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UF1404L-TA3-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) TA3: TO-220
	(3)Lead Free	(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	40	V
Gate-Source Voltage			V_{GSS}	± 20	V
Drain Current	Continuous ($V_{GS}=10\text{V}$)	$T_C=25^\circ\text{C}$	I_D	162 (Note 5)	A
		$T_C=100^\circ\text{C}$		115 (Note 5)	A
	Pulsed (Note 2)		$T_C=25^\circ\text{C}$	I_{DM}	650
Avalanche Current (Note 2)			I_{AR}	95	A
Avalanche Energy	Single Pulsed (Note 3)		E_{AS}	519	mJ
	Repetitive (Note 2)		E_{AR}	20	mJ
Peak Diode Recovery dv/dt (Note 3)			dv/dt	5.0	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)			P_D	200	W
Junction Temperature			T_J	+150	$^\circ\text{C}$
Storage Temperature			T_{STG}	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive rating: pulse width limited by maximum junction temperature

3. Starting $T_J=25^\circ\text{C}$, $L=0.12\text{mH}$, $R_G=25\Omega$, $I_{AS}=95\text{A}$

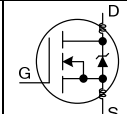
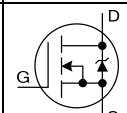
4. $I_{SD}\leq 95\text{A}$, $di/dt\leq 150\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, $T_J\leq 175^\circ\text{C}$

5. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

■ THERMAL CHARACTERISTICS

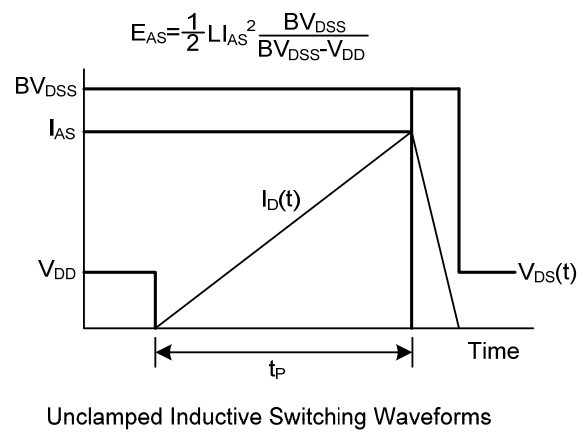
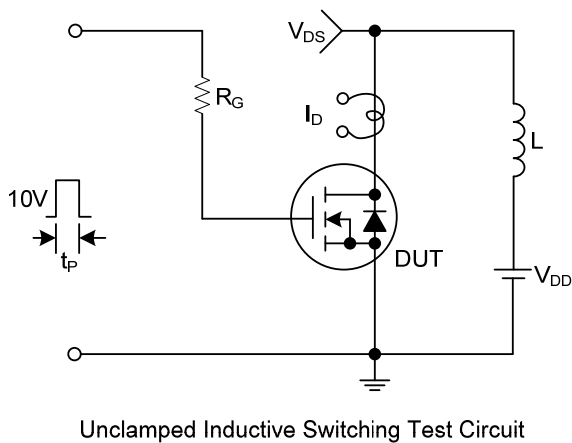
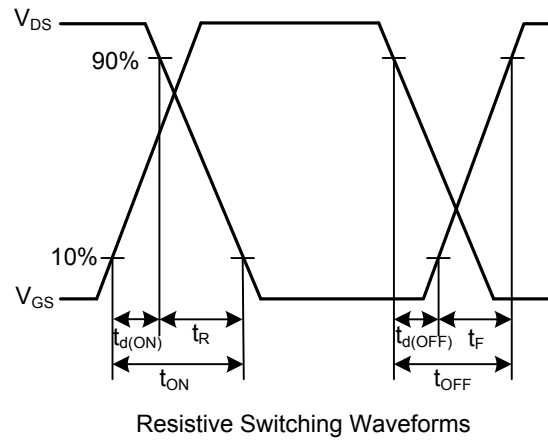
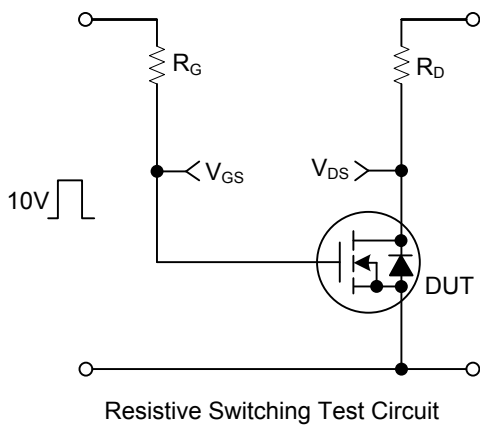
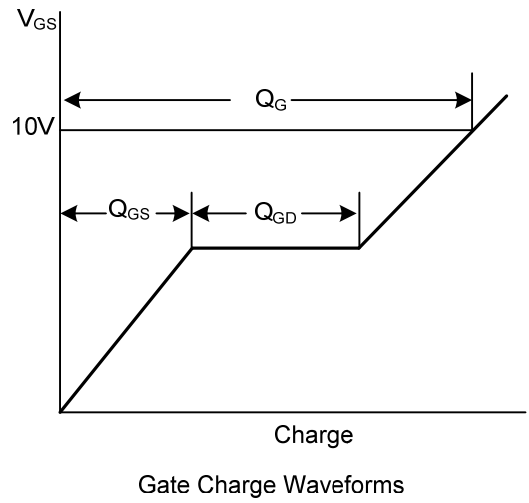
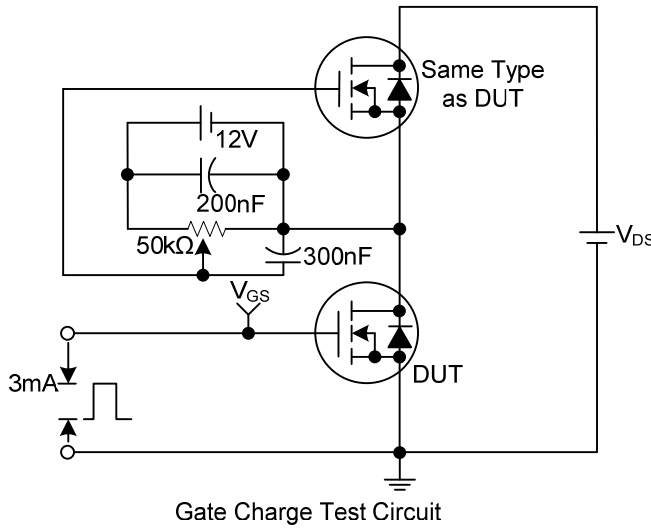
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.625	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

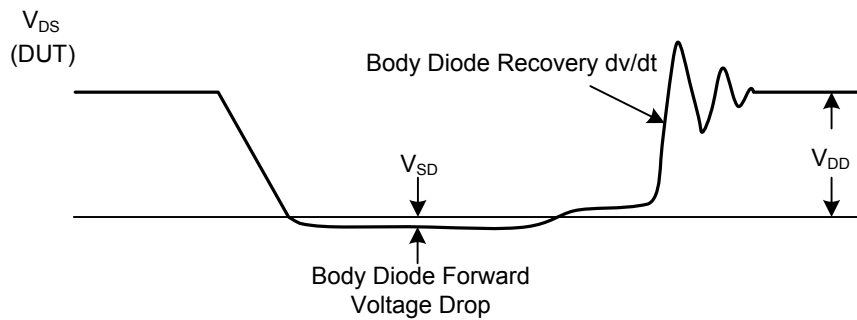
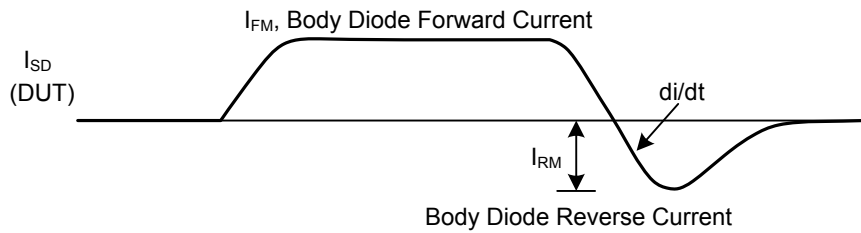
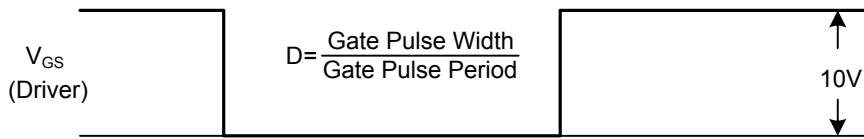
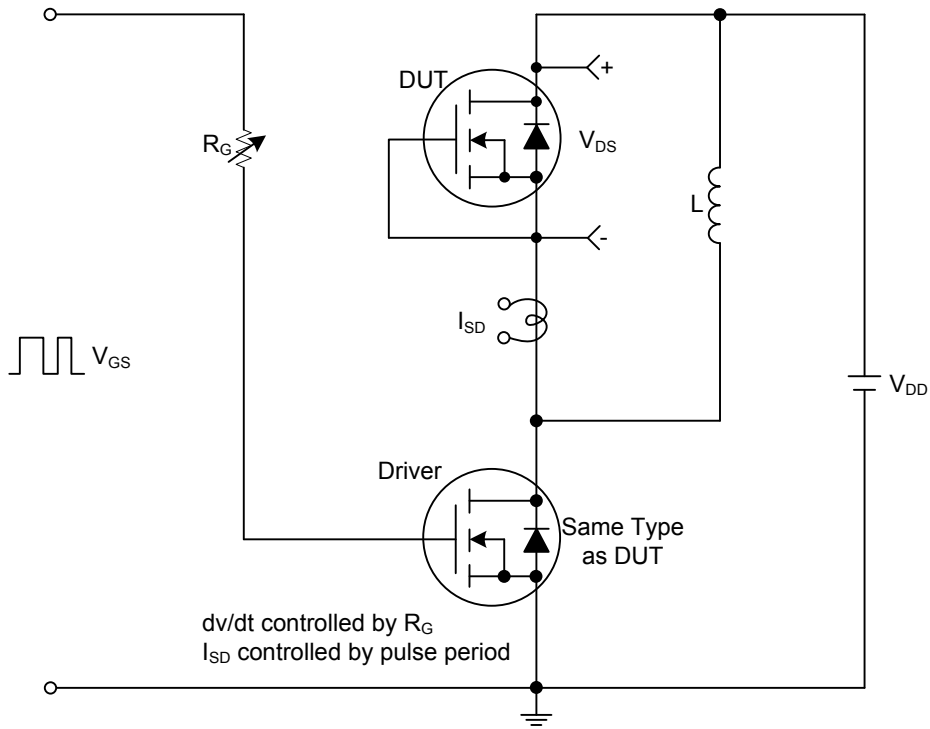
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	40			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =1mA		0.036		V/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			20	μA
		V _{DS} =32V, V _{GS} =0V, T _J =150°C			250	μA
Gate- Source Leakage Current	Forward	V _{GS} =+20V			+200	nA
	Reverse	V _{GS} =-20V			-200	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =95A (Note 2)		3.5	4	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		7.36		nF
Output Capacitance	C _{OSS}			1.68		nF
Reverse Transfer Capacitance	C _{RSS}			0.24		nF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	I _D =95A, V _{DS} =32V, V _{GS} =10V (Note 2)		160	200	nC
Gate to Source Charge	Q _{GS}			35		nC
Gate to Drain Charge	Q _{GD}			42	60	nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =20V, I _D =95A, R _G =2.5Ω, R _D =0.21Ω (Note 2)		17		ns
Rise Time	t _R			140		ns
Turn-OFF Delay Time	t _{D(OFF)}			72		ns
Fall-Time	t _F			26		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25in.) from package and center of die contact		4.5		nH
Internal Source Inductance	L _S			7.5		nH
Maximum Body-Diode Continuous Current (Note 4)	I _S	MOSFET symbol showing the integral reverse p-n junction diode.			162	A
Maximum Body-Diode Pulsed Current (Note 1)	I _{SM}				650	A
Drain-Source Diode Forward Voltage	V _{SD}	I _S =95A, V _{GS} =0V, T _J =25°C (Note 2)			1.3	V
Body Diode Reverse Recovery Time	t _{RR}	I _F =95A, di/dt=100A/μs,		71	110	ns
Body Diode Reverse Recovery Charge	Q _{RR}	T _J =25°C (Note 2)		180	270	μC

- Notes: 1. Repetitive rating: pulse width limited by maximum junction temperature
2. Pulse width ≤ 300μs, Duty cycle ≤ 2%
3. C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
4. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

■ TEST CIRCUITS AND WAVEFORMS



■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit and Waveforms

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