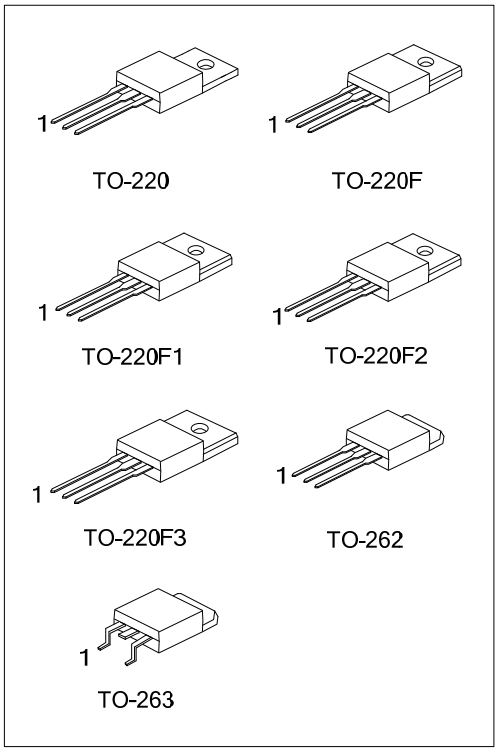
8A, 500V, 0.85Ω, N-CHANNEL POWER MOSFET



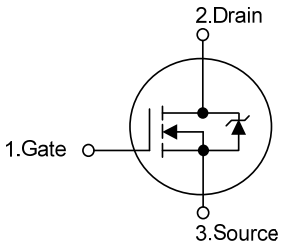
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ FEATURES

* Low $R_{DS(ON)}$< 0.85Ω @ V_{GS} = 10V
* Single Pulse Avalanche Energy Rated
* Fast Switching Speeds
* Linear Transfer Characteristics
* High Input Impedance

■ SYMBOL



■ ORDERING INFORMATION

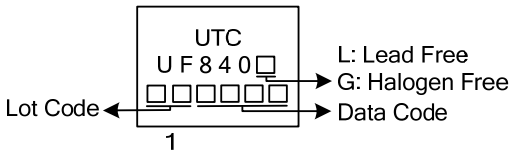
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF840L-TA3-T	UF840G-TA3-T	TO-220	G	D	S	Tube
UF840L-TF1-T	UF840G-TF1-T	TO-220F1	G	D	S	Tube
UF840L-TF2-T	UF840G-TF2-T	TO-220F2	G	D	S	Tube
UF840L-TF3-T	UF840G-TF3-T	TO-220F	G	D	S	Tube
UF840L-TF3T-T	UF840G-TF3T-T	TO-220F3	G	D	S	Tube
UF840L-T2Q-T	UF840G-T2Q-T	TO-262	G	D	S	Tube
UF840L-TQ2-T	UF840G-TQ2-T	TO-263	G	D	S	Tube
UF840L-TQ2-R	UF840G-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UF840L-TA3-T
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) T: Tube, R: Tape Reel
(2) TA3: TO-220, TF1: TO-220F1, TF2: TO-220F, TF3: TO-220F, TF3T: TO-220F3, T2Q: TO-262, TQ2: TO-263
(3) L: Lead Free, G: Halogen Free

■ MARKING INFORMATION

PACKAGE	MARKING
TO-220 TO-220F TO-220F1 TO-220F2 TO-220F3 TO-262 TO-263	

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless Otherwise Specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T_J =25°C ~125°C)		V_{DSS}	500	V
Drain to Gate Voltage (R_{GS} = 20kΩ, T_J =25°C ~125°C)		V_{DGR}	500	V
Gate to Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous	I_D	8.0	A
	Pulsed	I_{DM}	32	A
Power Dissipation (T_C=25°C)	TO-220	P_D	134	W
	TO-220F/TO-220F1 TO-220F3		44	
	TO-220F2		46	
	TO-262/TO-263		134	
Single Pulse Avalanche Energy		E_{AS}	510	mJ
Operating Temperature		T_{OPR}	-55 ~ +150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220	θ_{JC}	0.93	°C/W
	TO-220F/TO-220F1 TO-220F3		2.86	
	TO-220F2		2.72	
	TO-262/TO-263		0.93	

■ ELECTRICAL SPECIFICATIONS (T_A =25°C, unless Otherwise Specified.)

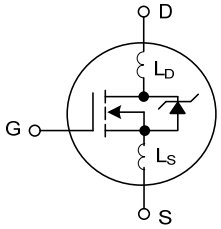
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	500			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D = 250μA	2		4	V
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)MAX}$, V_{GS}=10V	8			A
Drain-Source Leakage Current	I_{DSS}	V_{DS}=Rated BV_{DSS}, V_{GS} = 0V			25	μA
		V_{DS}=0.8xRated BV_{DSS},V_{GS}=0V,T_J= 125°C			250	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±30V			±100	nA
Static Drain-Source On-State Resistance (Note 1)	$R_{DS(ON)}$	V_{GS}=10V. I_D = 4.4A		0.73	0.85	Ω
Turn-On Delay Time	$t_{DLY(ON)}$	V_{DD}=30V, I_D ≈ 1A, R_G=9.1Ω, R_L =30Ω (Note 2)		60	70	ns
Turn-Off Delay Time	$t_{DLY(OFF)}$			260	300	ns
Turn-On Rise Time	t_R			60	70	ns
Turn-Off Fall Time	t_F			90	110	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} =10V, I_D =8A,V_{DS}=120V $I_{G(REF)}$ =3.3mA (Note 3)		116	120	nC
Gate-Source Charge	Q_{GS}			13		nC
Gate-Drain Charge	Q_{GD}			22		nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz		750		pF
Output Capacitance	C_{OSS}			130		pF
Reverse Transfer Capacitance	C_{RSS}			16		pF

Note : 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.
3. Gate Charge is Essentially Independent of Operating Temperature.

■ INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DRAIN INDUCTANCE					
Measured from the contact screw on tab to center of die	L_D		3.5		nH
Measured from the drain lead(6mm from package) to center of die			4.5		nH
SOURCE INDUCTANCE					
Measured from the source lead(6mm from header) to source bond pad	L_S		7.5		nH

Remark: Modified MOSFET symbol showing the internal devices inductances as below.

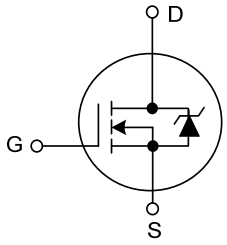


■ SOURCE TO DRAIN DIODE SPECIFICATIONS

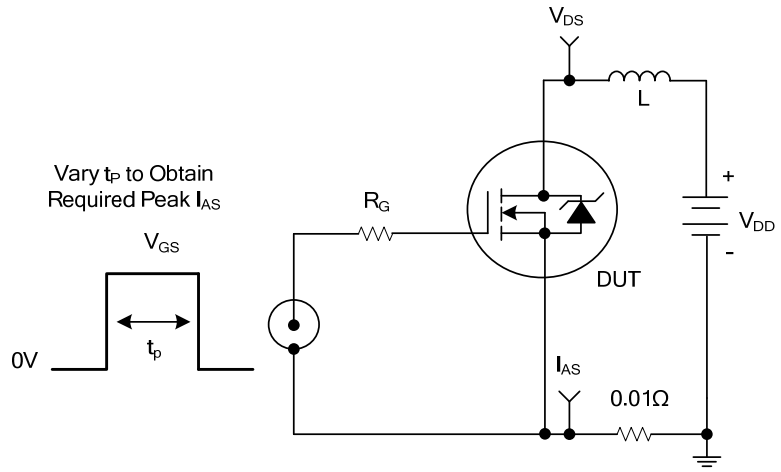
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage(Note 1)	V_{SD}	T_J = 25°C, I_{SD} = 8.0A, V_{GS} = 0V			2	V
Continuous Source to Drain Current	I_{SD}	Note 2			8	A
Pulse Source to Drain Current	I_{SDM}				32	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_{SD} = 8.0A, dI_{SD}/dt = 100A/μs	210	475	970	ns
Reverse Recovery Charge	Q_{RR}	T_J = 25°C, I_{SD} = 8.0A, dI_{SD}/dt = 100A/μs	2	4.6	8.2	μC

Notes: 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.

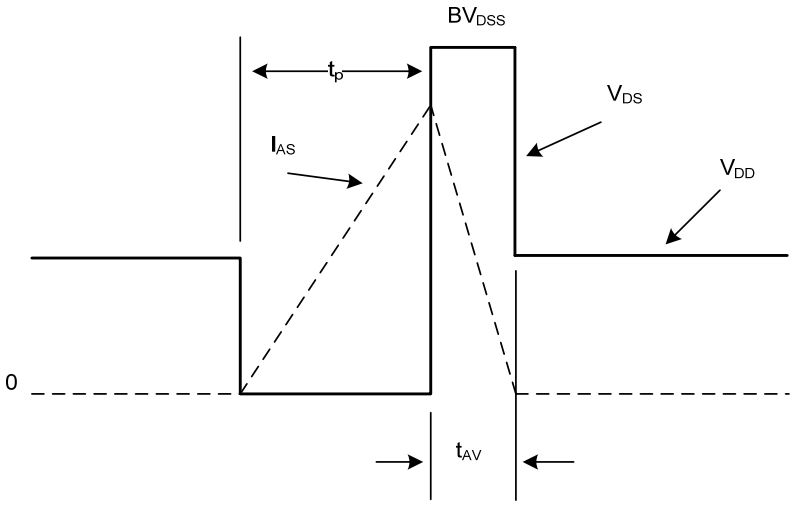
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



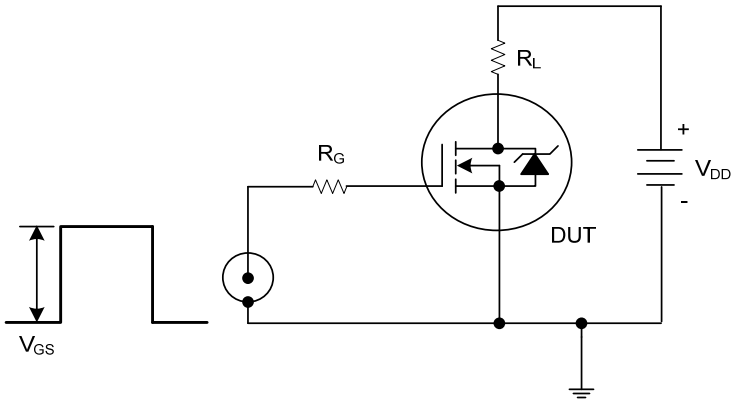
■ TEST CIRCUITS AND WAVEFORMS



Unclamped Energy Test Circuit

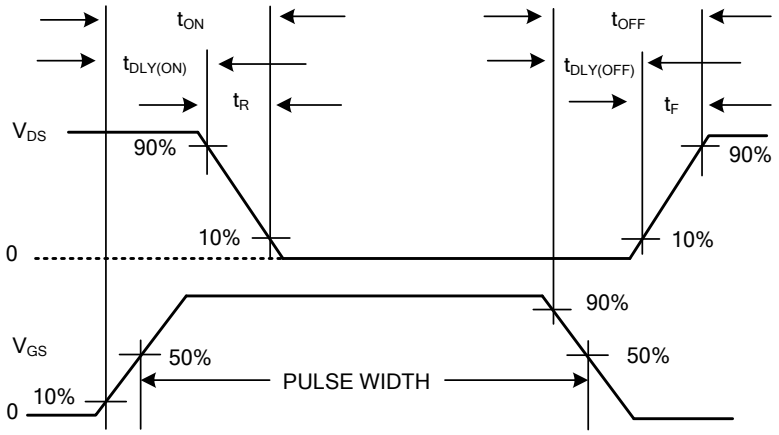


Unclamped Energy Waveforms

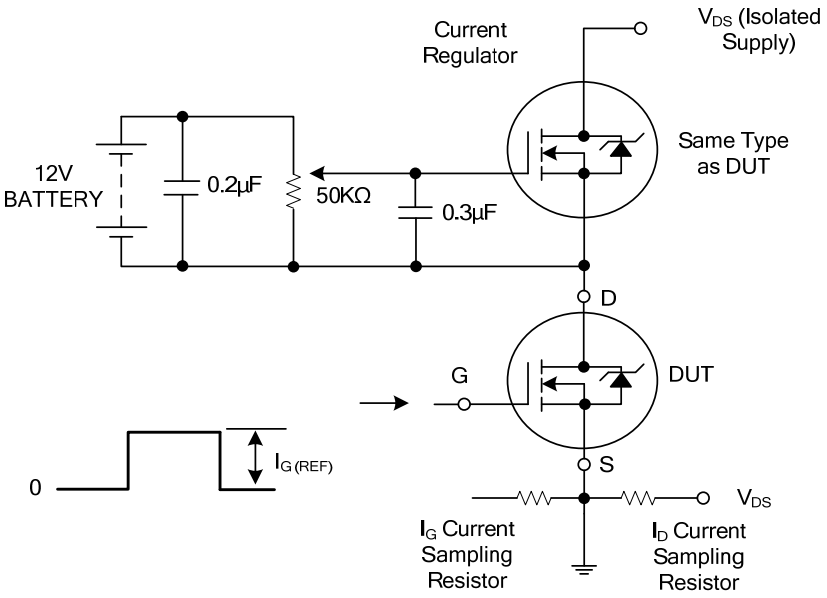


Switching Time Test Circuit

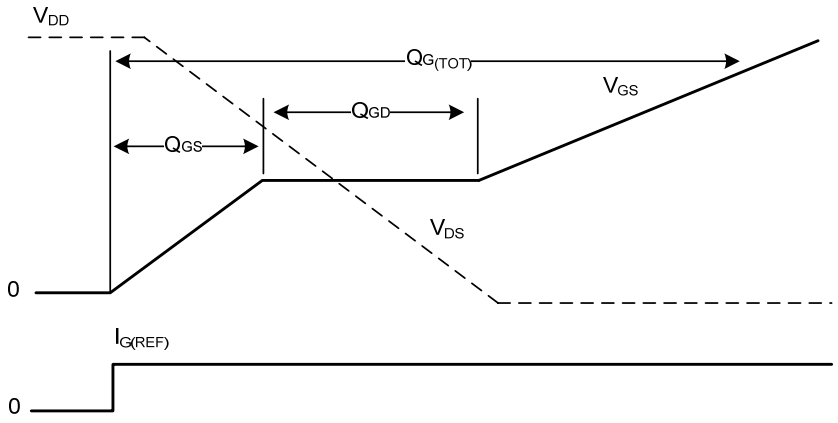
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



Resistive Switching Waveforms



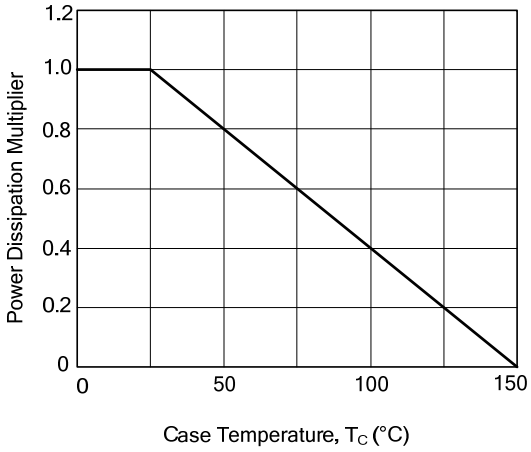
Gate Charge Test Circuit



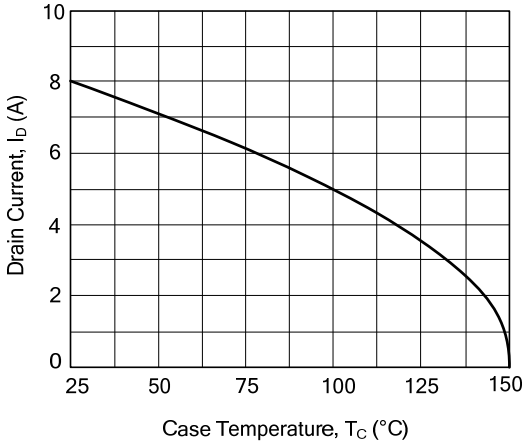
Gate Charge Waveforms

■ TYPICAL CHARACTERISTICS

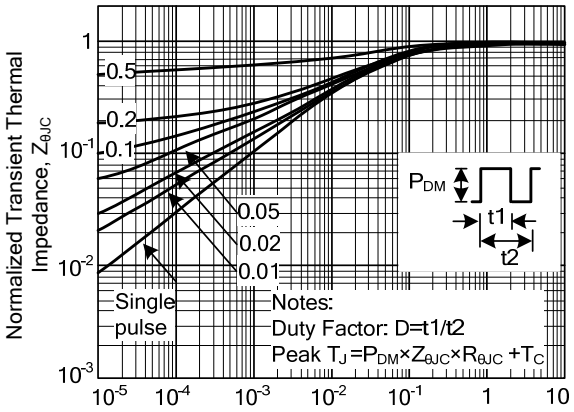
Normalized Power Dissipation vs. CaseTemperature



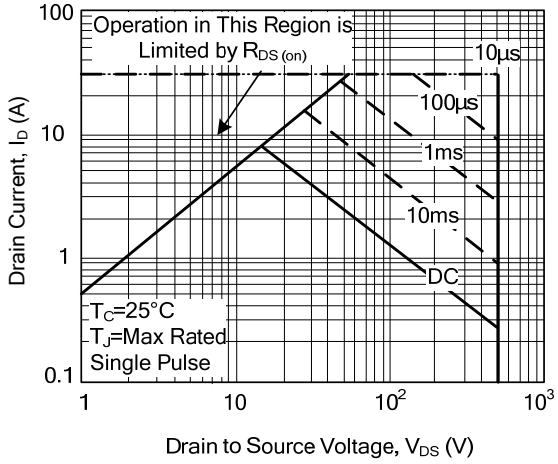
Maximum Contionuous Drain Current vs. Case Temperature



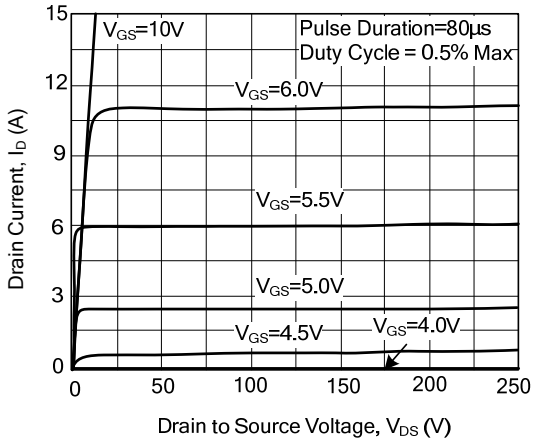
Normalized Maximum Transient Thermal Impedance



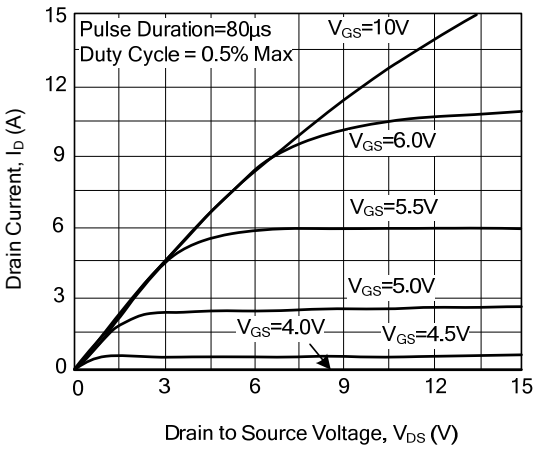
Forward Bias Safe Operating Area



Output Characteristics

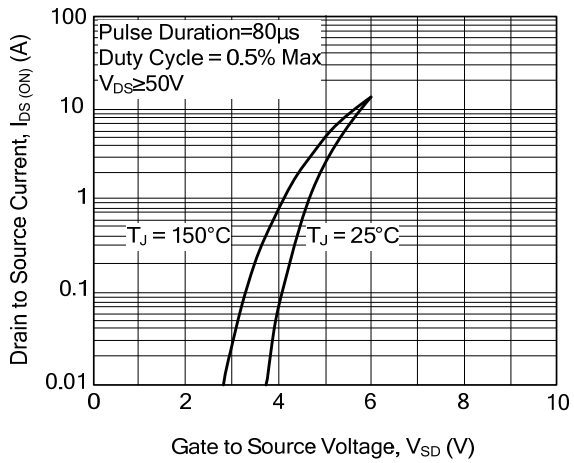


Saturation Characteristics

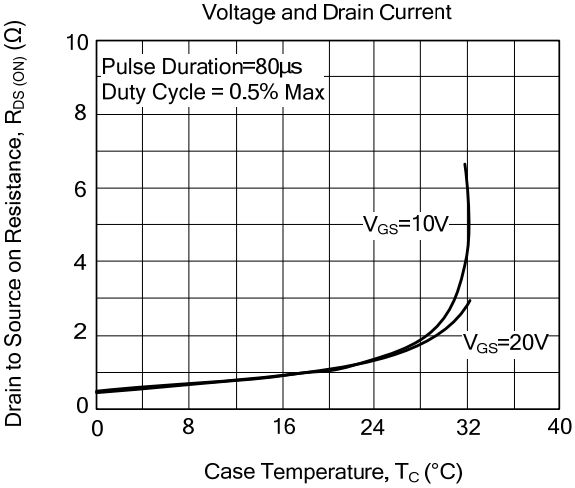


■ TYPICAL CHARACTERISTICS(Cont.)

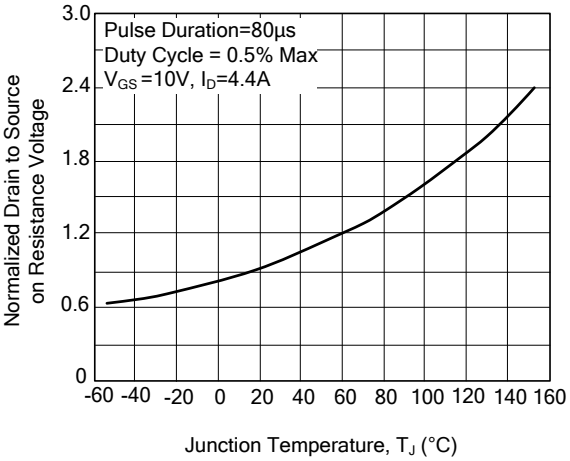
Transfer Characteristics



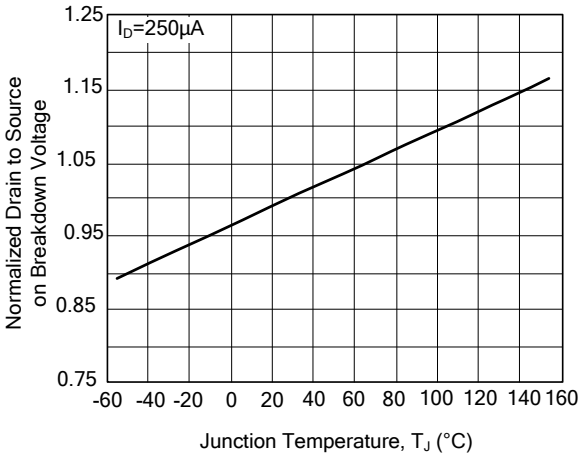
Drain to Source on Resistance vs. Voltage and Drain Current



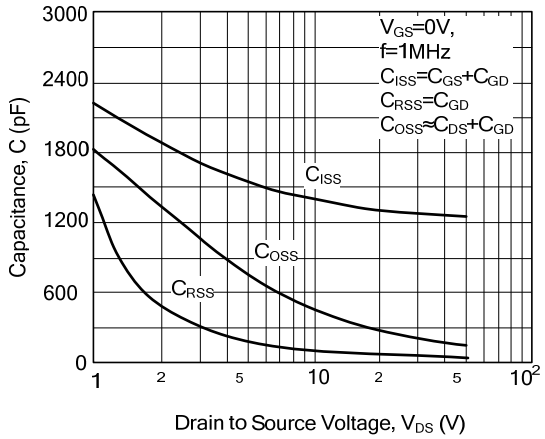
Normalized Drain to Source on Resistance vs. Junction Temperature



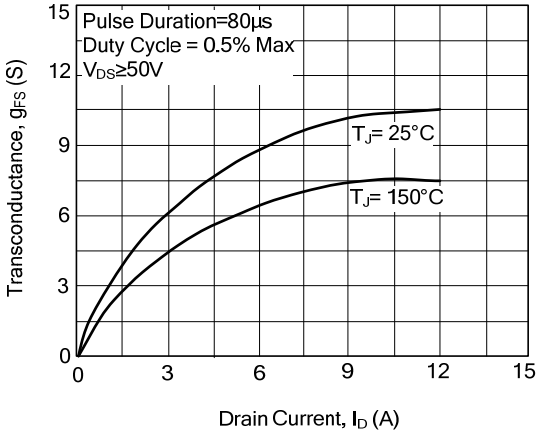
Normalized Drain to Source Breakdown Voltage vs. Junction Temperature



Capacitance vs. Drain to Source Voltage

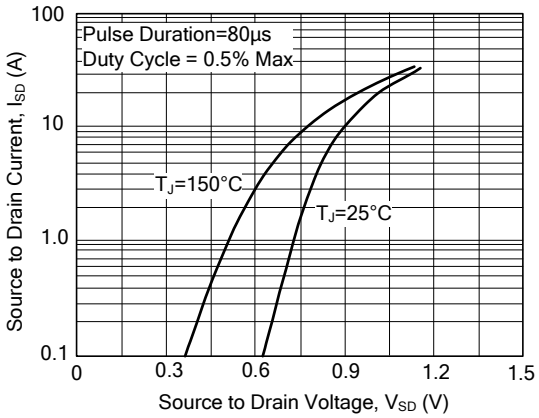


Transconductance vs. Drain Current



■ TYPICAL CHARACTERISTICS(Cont.)

Source to Drain DIODE Voltage



Gate to Source Voltage vs. Gate Charge