

N-Channel 40V(D-S) MOSFET

GENERAL DESCRIPTION

The PT G-FI is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leq 40m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 65m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

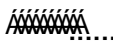
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Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V

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Electrical Characteristics ($T_j=25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	40			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	1.0		3.0	V
I _{GSS}	Gate Body Leakage	V _{DS} =0V, V _{GS} = \pm 20V			\pm 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =10V, I _D = 4.0A		32	40	m Ω
		V _{GS} =4.5V, I _D = 3.5A		50	65	
V _{SD}	Diode Forward Voltage	I _S =1A		0.8	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =10V, I _D =4A		16		nC
Q _g	Total Gate Charge	V _{DS} =20V, V _{GS} =4.5V, I _D =4A		8.2		
Q _{gs}	Gate-Source Charge			3.6		
Q _{gd}	Gate-Drain Charge			3.9		
C _{iss}	Input capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz		560		pF
C _{oss}	Output Capacitance			70		
C _{rss}	Reverse Transfer Capacitance			22		
R _g	Gate Resistance	f =1MHz		0.7		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =20V, R _L =20 Ω I _D =1A, V _{GEN} =10V R _G =1 Ω		12		ns
t _r	Turn-On Rise Time			12		
t _{d(off)}	Turn-Off Delay Time			37		
t _f	Turn-Off Fall Time			4		

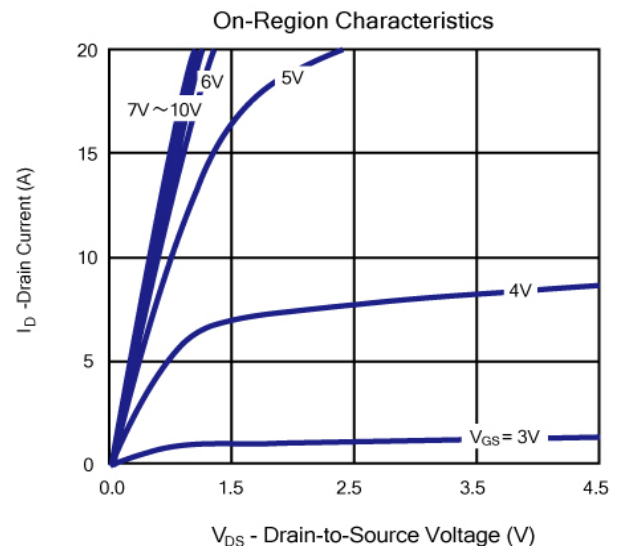
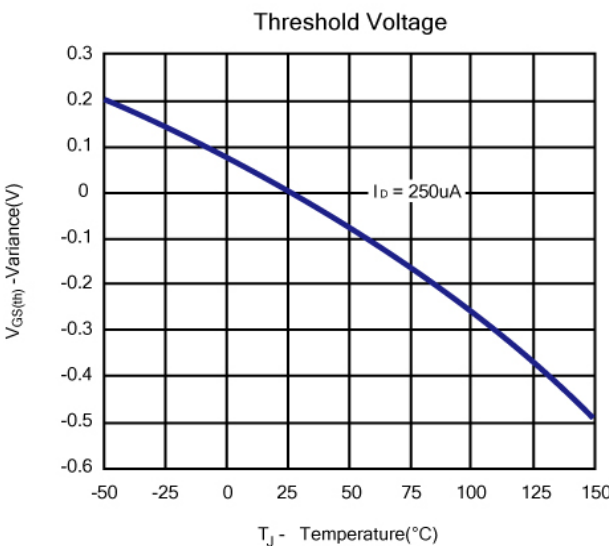
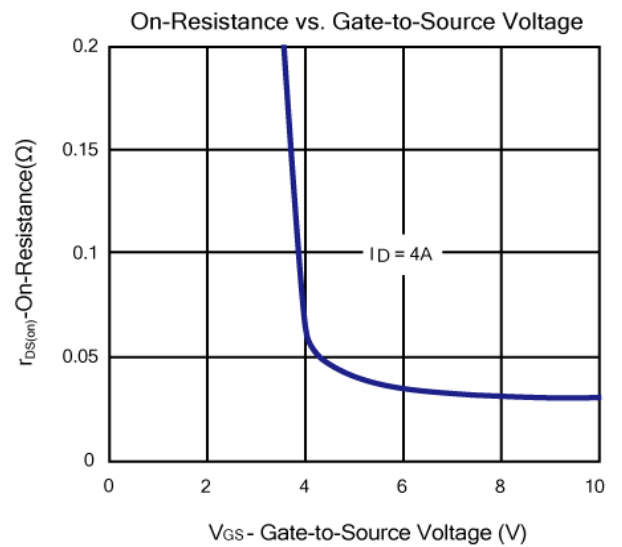
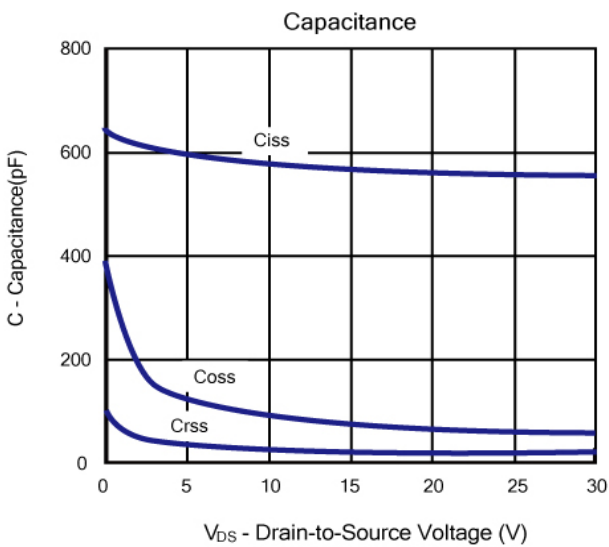
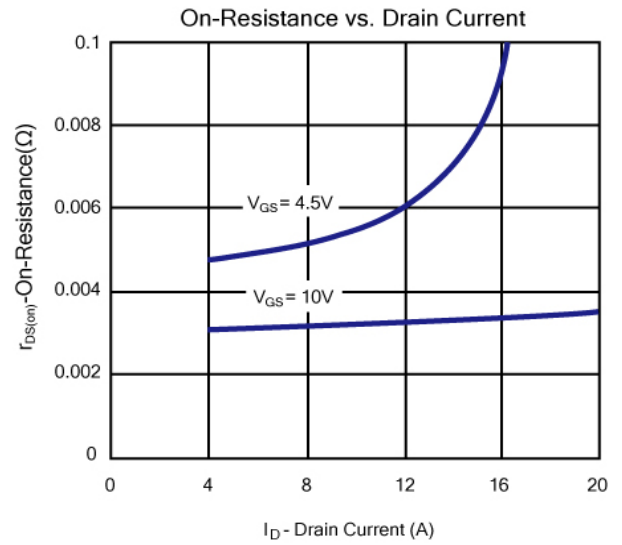
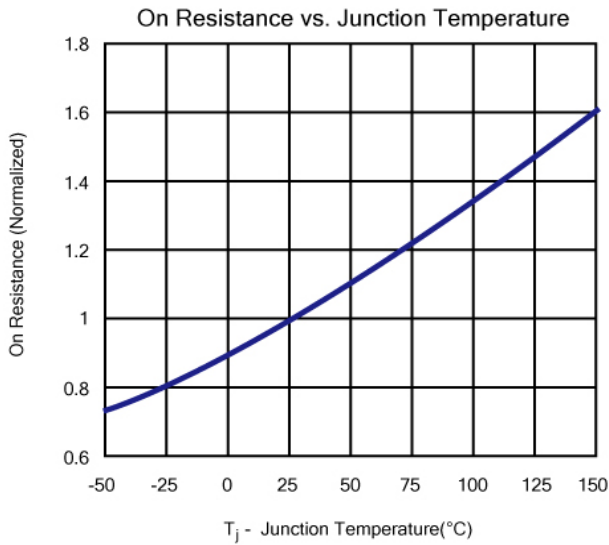
Notes: a. Based on epoxy or solder paste and bond wire Cu 2mil \times 3(S), Au 1mil \times 1(G) on each die of SOT-23 package.

b. Pulse test; pulse width \leq 300us, duty cycle \leq 2%.

c. H&M SEMI reserves the right to improve product design, functions and reliability without notice.

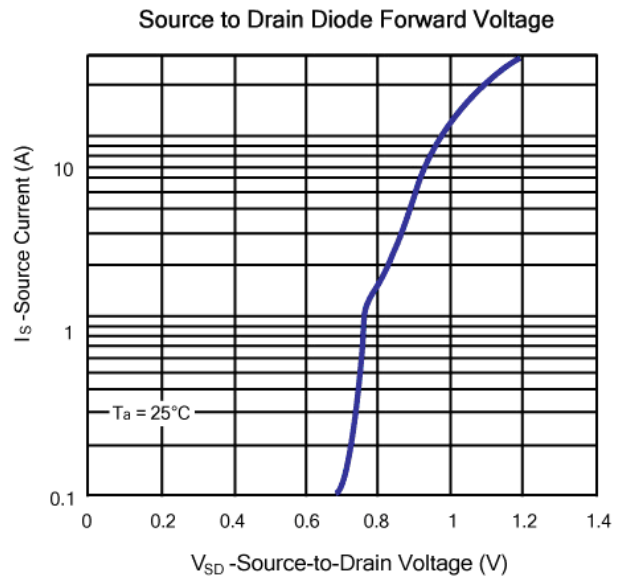
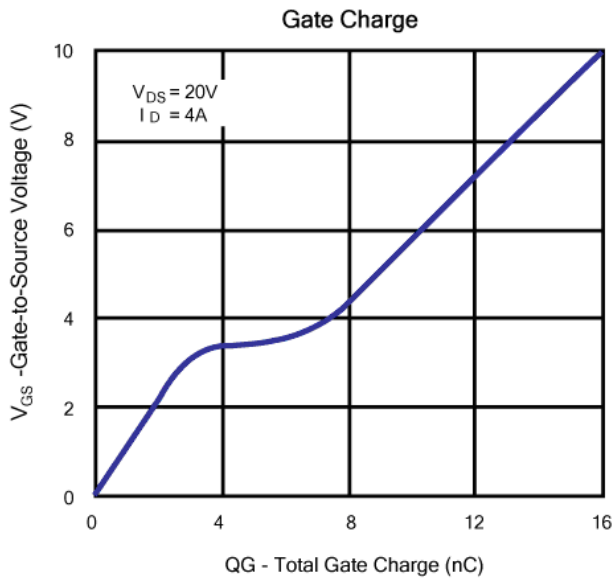
Typical Characteristics (T_J =25°C Noted)

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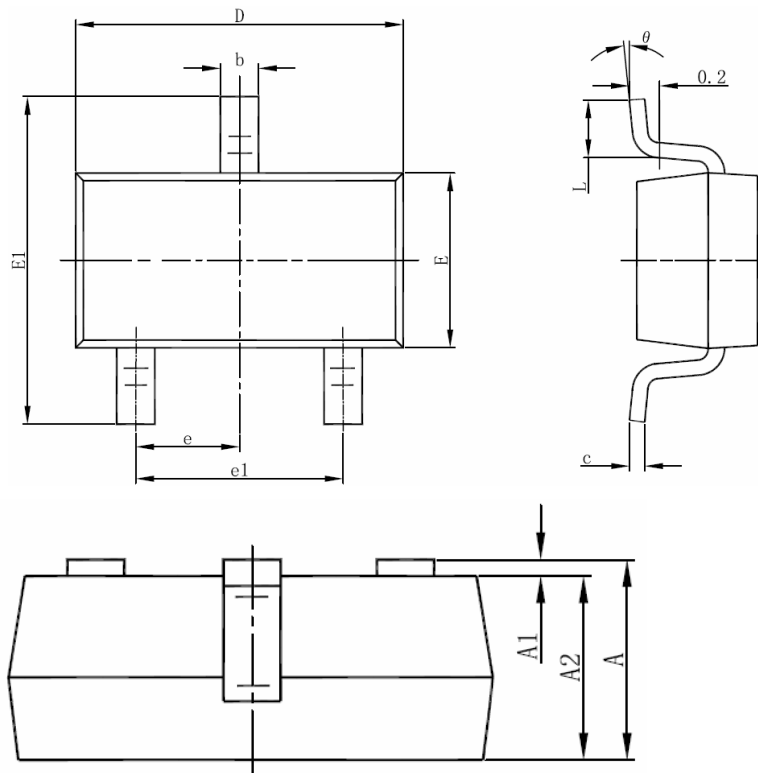


Typical Characteristics (T_J = 25°C Noted)

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SOT-23-3L PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTES

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.