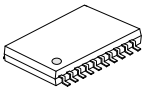
U74HC377

CMOS IC

OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE



SOP-20

TSSOP-20

■ DESCRIPTION

The device is positive-edge-triggered octal D-type flip-flops with an enable input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse, if $\overline{EN}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at $\overline{EN}$.

■ FEATURES

* Wide Operating Voltage Range of 2V to 6V
* Outputs Can Drive Up To 10 LSTTL Loads
* Low Power Consumption, I_{CC}=8μA (Max.)
* Typical t_{PD}=12ns
* ±4mA Output Drive at 5V
* Low Input Current of 1μA Max.
* Eight Flip-Flops With Single-Rail Outputs
* Clock Enable Latched to Avoid False Clocking
* Applications Include
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

■ ORDERING INFORMATION

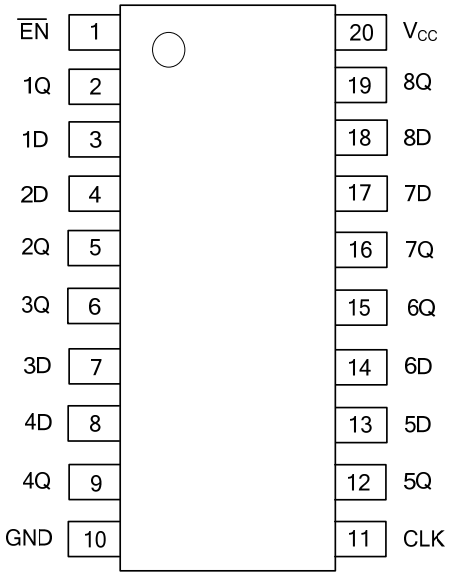
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC377L-S20-T	U74HC377G-S20-T	SOP-20	Tube
U74HC377L-S20-R	U74HC377G-S20-R	SOP-20	Tape Reel
U74HC377L-P20-T	U74HC377G-P20-T	TSSOP-20	Tube
U74HC377L-P20-R	U74HC377G-P20-R	TSSOP-20	Tape Reel

U74HC377L-P20-T

(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) T: Tube, R: Tape Reel
(2) P20: TSSOP-20, S20: SOP-20
(3) L: Lead Free, G: Halogen Free

■ PIN CONFIGURATION



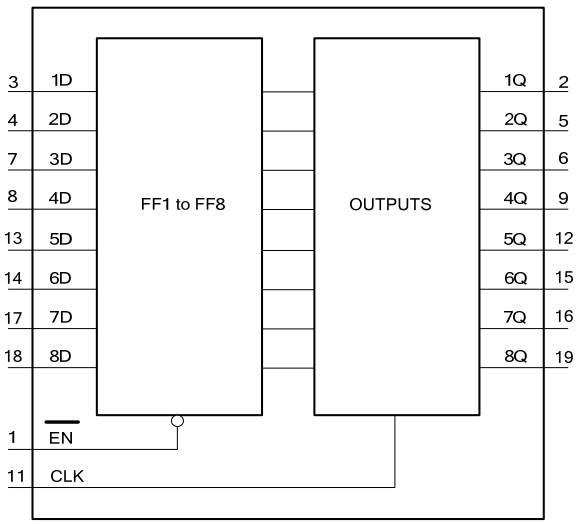
■ PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
$\overline{EN}$	1	Data Enable Input (Active low)
1Q	2	Flip-flop Output
1D	3	Data Input
2D	4	Data Input
2Q	5	Flip-flop Output
3Q	6	Flip-flop Output
3D	7	Data Input
4D	8	Data Input
4Q	9	Flip-flop Output
GND	10	Ground (0V)
CLK	11	Clock Input (Low-to-High, Edge Triggered)
5Q	12	Flip-flop Output
5D	13	Data Input
6D	14	Data Input
6Q	15	Flip-Flop Output
7D	16	Flip-Flop Output
7Q	17	Data Input
8D	18	Data Input
8Q	19	Flip-Flop Output
V_{CC}	20	Supply Voltage

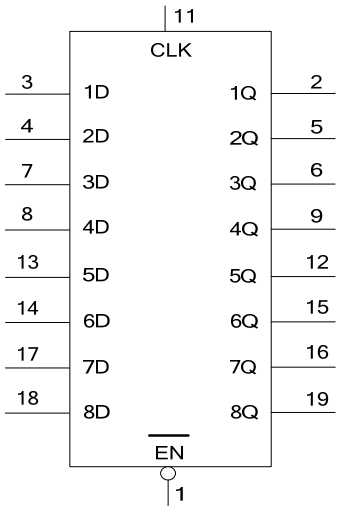
■ FUNCTION TABLE

INPUTS			OUTPUT Q
$\overline{EN}$	CLK	D	
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

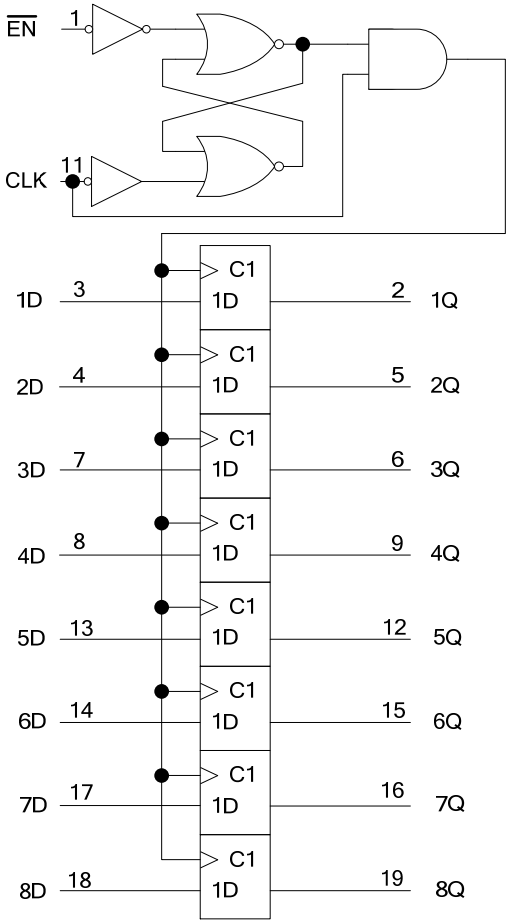
■ FUNCTIONAL DIAGRAM



■ LOGIC SYMBOL



■ LOGIC DIAGRAM (POSITIVE LOGIC)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
V_{CC} or GND Current	I_{CC}	±50	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
High-level Input Voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			
		V_{CC}=6V	4.2			
Low-level Input Voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	
		V_{CC}=6V			1.8	
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise/Fall Time	△t/△v	V_{CC}=2V			1000	ns
		V_{CC}=4.5V			500	
		V_{CC}=6V			400	
Operating Free-air Temperature	T_A		-40		+85	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-20	θ_{JA}	58	°C/W
	TSSOP-20		83	

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	1.998		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		
		V_{CC}=6V, I_{OH}=-20μA	5.9	5.999		
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.3		
		V_{CC}=6V, I_{OH}=-5.2mA	5.48	5.8		
Output Voltage Low-Level	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1	
		V_{CC}=4.5V, I_{OL}=4mA		0.17	0.26	
		V_{CC}=6V, I_{OL}=5.2mA		0.15	0.26	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}= V_{CC} or GND		±0.1	±100	nA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8	μA
Input Capacitance	C_I	V_{CC}=2V to 6V		3	10	pF

■ TIMING REQUIREMENTS (T_A =25°C , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency		f_{CLOCK}	V_{CC}=2.0V			5	MHz
			V_{CC}=4.5V			25	MHz
			V_{CC}=6.0V			29	MHz
Pulse duration	CLK high or low	t_W	V_{CC}=2.0V	100			ns
			V_{CC}=4.5V	20			ns
			V_{CC}=6.0V	17			ns
Setup time before CLK↑	D	t_{SU}	V_{CC}=2.0V	100			ns
			V_{CC}=4.5V	20			ns
			V_{CC}=6.0V	17			ns
	$\overline{EN}$ high or low		V_{CC}=2.0V	100			ns
			V_{CC}=4.5V	20			ns
			V_{CC}=6.0V	17			ns
Hold time after CLK↑	$\overline{EN}$ inactive or active, data	t_H	V_{CC}=2.0V	5			ns
			V_{CC}=4.5V	5			ns
			V_{CC}=6.0V	5			ns

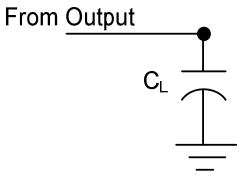
■ SWITCHING CHARACTERISTICS (t_r= t_f= 6ns, C_L=50pF, T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum Frequency Response	f_{MAX}	V_{CC}=2.0V	5	11		ns
		V_{CC}=4.5V	25	54		ns
		V_{CC}=6.0V	29	64		ns
From CLK to Q	t_{PD}	V_{CC}=2.0V		56	160	ns
		V_{CC}=4.5V		15	32	ns
		V_{CC}=6.0V		12	27	ns
To Any	t_t	V_{CC}=2.0V		38	75	ns
		V_{CC}=4.5V		8	15	ns
		V_{CC}=6.0V		6	13	ns

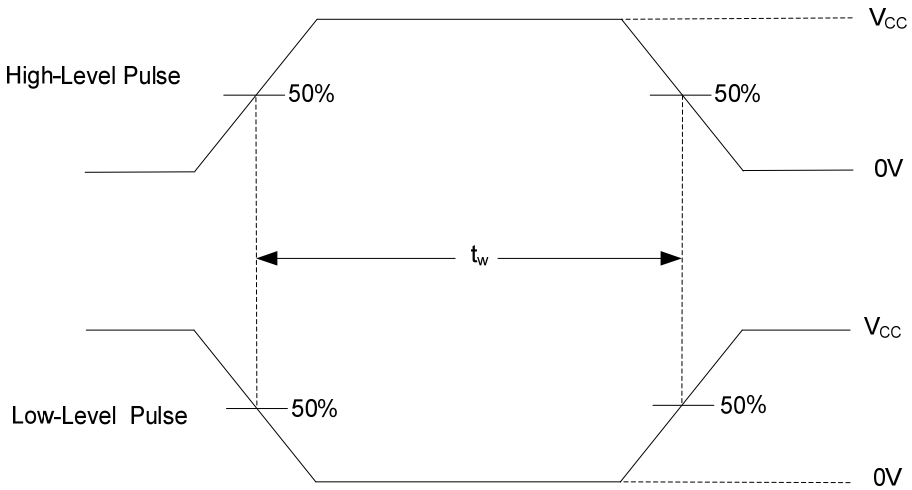
■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load.		30		pF

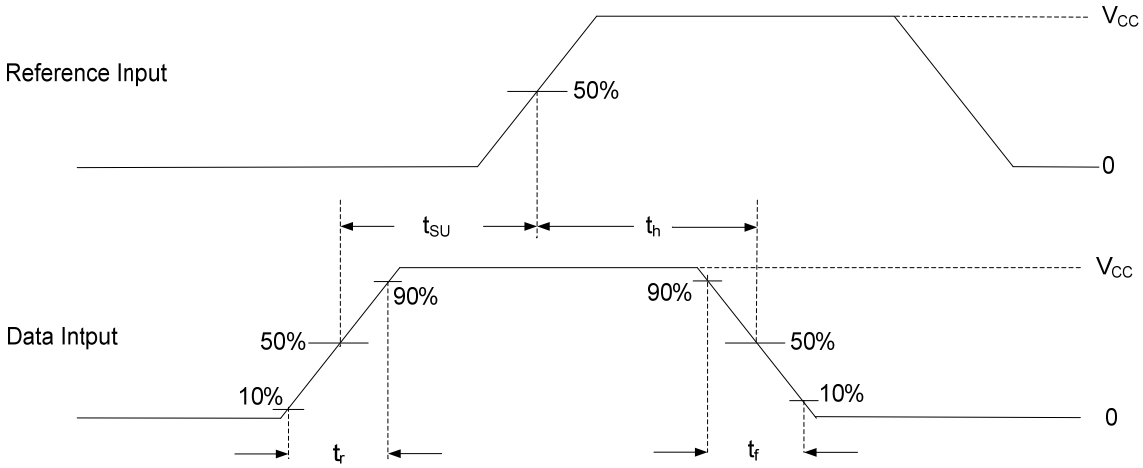
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

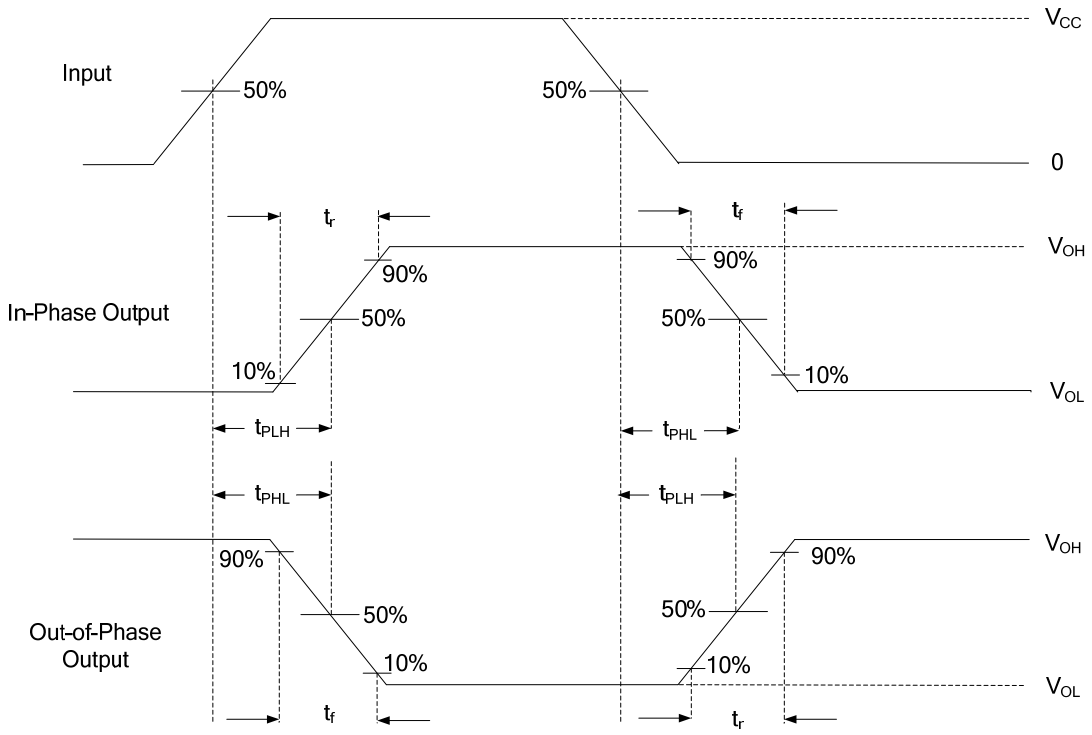


PULSE DURATIONS



SETUP AND HOLD AND INPUT RISE AND FALL TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Notes: A. C_L includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulse are supplied by generators having the following characteristics: PRR≤1MHz, Z_O=50Ω.

C. For clock inputs, f_{MAX} is measured when the input duty cycle is 50%.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{PD}.