

# U74LVC1G74

**CMOS IC**

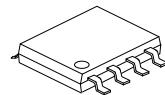
## SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

### ■ DESCRIPTION

This single positive-edge-triggered D-type flip-flop is designed for 1.65V to 5.5V V<sub>CC</sub> operation.

A low level at the preset( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) input sets or resets the outputs, regardless of the levels of the other inputs .when  $\overline{PRE}$  and  $\overline{CLR}$  are inactive(high),data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



SOP-8

### ■ FEATURES

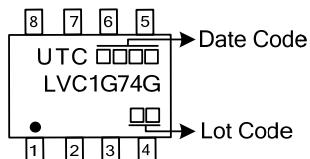
- \* Supports 5-V V<sub>CC</sub> operation
- \* Inputs accept voltages to 5.5V
- \* Max t<sub>pd</sub> of 5.9ns at 3.3V
- \* Typical V<sub>OOLP</sub><0.8V at V<sub>CC</sub>=3.3V, T<sub>A</sub>=25°C
- \* Typical V<sub>OOLV</sub>>2V at V<sub>CC</sub>=3.3V, T<sub>A</sub>=25°C
- \* Low Power Consumption, I<sub>CC</sub>=10µA (Max.)
- \* I<sub>off</sub> Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection

### ■ ORDERING INFORMATION

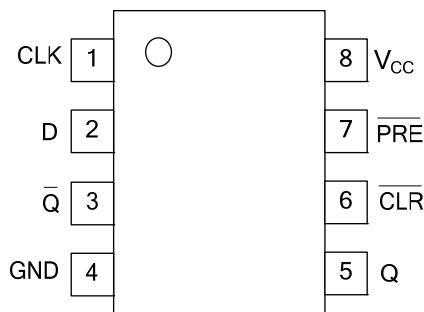
Ordering Number	Package	Packing
U74LVC1G74G-S08-R	SOP-8	Tape Reel

U74LVC1G74G-S08-R 	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free
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■ MARKING



■ PIN CONFIGURATION

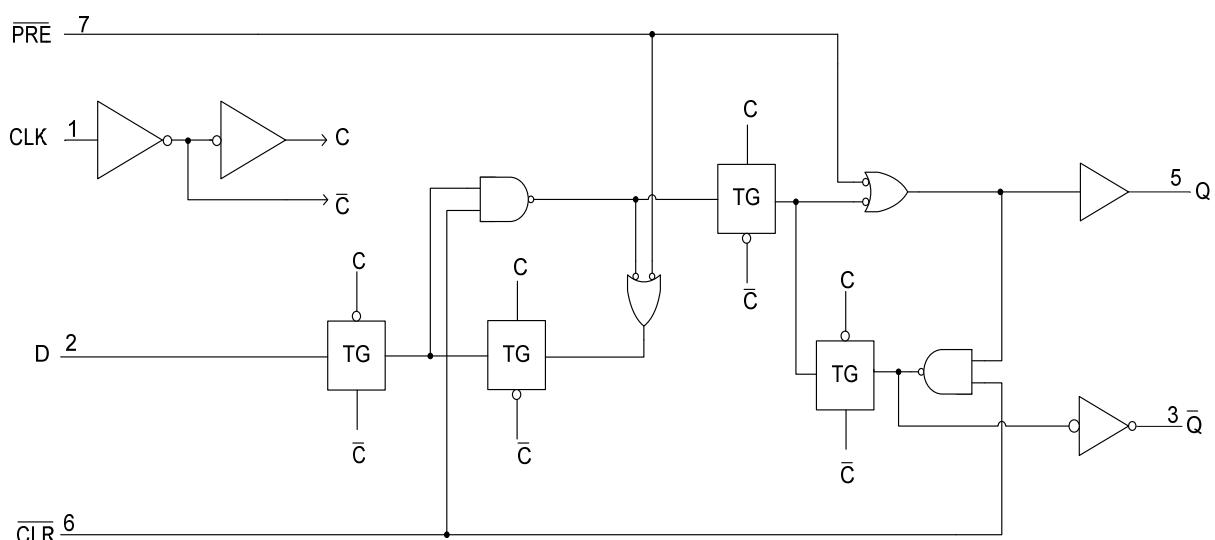


■ FUNCTION TABLE

INPUTS			OUTPUT		
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H *	H *
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}_0$

\* This configuration is unstable, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to high level.

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sub>CC</sub>	-0.5~6.5	V
Input Voltage	V <sub>IN</sub>	-0.5~ 6.5	V
Voltage range applied to any output in the high-impedance or power-off state	V <sub>OUT</sub>	-0.5~ 6.5	V
Voltage range applied to any output in the high or low state	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> +0.5	V
Input Clamp Current(V <sub>IN</sub> <0)	I <sub>IK</sub>	-50	mA
Output Clamp Current(V <sub>OUT</sub> <0)	I <sub>OK</sub>	-50	mA
Output Current	I <sub>OUT</sub>	±50	mA
V <sub>CC</sub> or GND Current	I <sub>CC</sub>	±100	mA
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V <sub>CC</sub>		1.65		5.5	V
Input Voltage	V <sub>IN</sub>		0		5.5	V
Output Voltage	V <sub>OUT</sub>		0		V <sub>CC</sub>	V
High-level input voltage	V <sub>IH</sub>	V <sub>CC</sub> =1.65V to 1.95V	0.65×V <sub>CC</sub>			V
		V <sub>CC</sub> =2.3V to 2.7V	1.7			
		V <sub>CC</sub> =3V to 3.6V	2			
		V <sub>CC</sub> =4.5V to 5.5V	0.7×V <sub>CC</sub>			
Low-level input voltage	V <sub>IL</sub>	V <sub>CC</sub> =1.65V to 1.95V			0.35×V <sub>CC</sub>	V
		V <sub>CC</sub> =2.3V to 2.7V			0.7	
		V <sub>CC</sub> =3V to 3.6V			0.8	
		V <sub>CC</sub> =4.5V to 5.5V			0.3×V <sub>CC</sub>	
High-level Output Current	I <sub>OH</sub>	V <sub>CC</sub> =1.65V			-4	mA
		V <sub>CC</sub> =2.3V			-8	
		V <sub>CC</sub> =3V			-16	
		V <sub>CC</sub> =4.5V			-24	
Low-level Output Current	I <sub>OL</sub>	V <sub>CC</sub> =1.65V			-32	mA
		V <sub>CC</sub> =2.3V			4	
		V <sub>CC</sub> =3V			8	
		V <sub>CC</sub> =4.5V			16	
Input Transition Rise or Fall Rate	Δt/Δv	V <sub>CC</sub> =3V			24	ns/V
		V <sub>CC</sub> =4.5V			32	
		V <sub>CC</sub> =1.8V±0.15V, 2.5V±0.2V			20	
		V <sub>CC</sub> =3.3V±0.3V, 5V±0.5V,			10	
Operating Temperature	T <sub>A</sub>		-40		+85	°C

Note: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

## ■ STATIC CHARACTERISTICS

(All typical values are at  $V_{CC}=3.3V$ ,  $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	$V_{OH}$	$V_{CC}=1.65V$ to $5.5V$ , $I_{OH}=-100\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=1.65V$ , $I_{OH}=-4mA$	1.2			
		$V_{CC}=2.3V$ , $I_{OH}=-8mA$	1.9			
		$V_{CC}=3V$	$I_{OH}=-16mA$	2.4		
			$I_{OH}=-24mA$	2.3		
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=4.5V$ , $I_{OH}=-32mA$	3.8			V
		$V_{CC}=1.65V$ to $5.5V$ , $I_{OL}=100\mu A$			0.1	
		$V_{CC}=1.65V$ , $I_{OL}=4mA$			0.45	
		$V_{CC}=2.3V$ , $I_{OL}=8mA$			0.3	
		$V_{CC}=3V$	$I_{OL}=16mA$		0.4	
Input Leakage Current	$I_{(LEAK)}$	$I_{OL}=24mA$			0.55	$\mu A$
		$V_{CC}=4.5V$ , $I_{OH}=32mA$			0.55	
		$V_{CC}=0V$ ~ $5.5V$ , $V_{IN}=5.5V$ or GND			$\pm 5$	
		$V_{CC}=0V$ , $V_{IN}$ or $V_{OUT}=5.5V$			$\pm 10$	
		$V_{CC}=1.65V$ to $5.5V$ , $V_{IN}=5.5V$ or GND $I_{OUT}=0$			10	
Quiescent Supply Current	$I_Q$					$\mu A$
Additional Quiescent Supply Current Per Input Pin	$\Delta I_Q$	$V_{CC}=3V$ to $5.5V$ , One input at $V_{CC}-0.6V$ , Other inputs at $V_{CC}$ or GND			500	$\mu A$
Input Capacitance	$C_{IN}$	$V_{CC}=3.3V$ , $V_{IN}=V_{CC}$ or GND		5		pF

## ■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency	$f_{clock}$	$V_{CC}=1.8V$			80	MHz
		$V_{CC}=2.5V$			175	MHz
		$V_{CC}=3.3V$			175	MHz
		$V_{CC}=5.0V$			200	MHz
Pulse duration	$t_w$	$V_{CC}=1.8V$	CLK	6.2		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	6.2		ns
		$V_{CC}=2.5V$	CLK	2.7		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	2.7		ns
		$V_{CC}=3.3V$	CLK	2.7		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	2.7		ns
		$V_{CC}=5.0V$	CLK	2		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	2		ns
Setup time before CLK↑ from Data to $\overline{PRE}$ or $\overline{CLR}$ inactive	$t_{su}$	$V_{CC}=1.8V$	CLK	2.9		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	1.9		ns
		$V_{CC}=2.5V$	CLK	1.7		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	1.4		ns
		$V_{CC}=3.3V$	CLK	1.3		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	1.2		ns
		$V_{CC}=5.0V$	CLK	1.1		ns
			$\overline{PRE}$ or $\overline{CLR}$ Low	1.0		ns
Hold time, data after CLK↑	$t_h$	$V_{CC}=1.8V$	0			ns
		$V_{CC}=2.5V$	0.3			ns
		$V_{CC}=3.3V$	1.2			ns
		$V_{CC}=5.0V$	0.5			ns

■ SWITCHING CHARACTERISTICS (See Fig. 1 and Fig. 2 for test circuit and waveforms.)

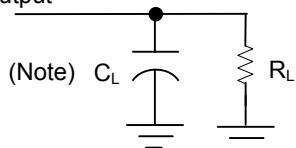
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum Frequency Response	$f_{Max}$	$V_{CC}=1.8V$	80			MHz
		$V_{CC}=2.5V$	175			MHz
		$V_{CC}=3.3V$	175			MHz
		$V_{CC}=5.0V$	200			MHz
Propagation delay from input (CLK) to output(Q)	$t_{PLH}/t_{PHL}$	$V_{CC}=1.8V$	4.8		13.4	ns
		$V_{CC}=2.5V$	2.2		7.1	ns
		$V_{CC}=3.3V$	2.2		5.9	ns
		$V_{CC}=5.0V$	1.4		4.1	ns
Propagation delay from input (CLK) to output( $\bar{Q}$ )	$t_{PLH}/t_{PHL}$	$V_{CC}=1.8V$	6		14.4	ns
		$V_{CC}=2.5V$	3		7.7	ns
		$V_{CC}=3.3V$	2.6		6.2	ns
		$V_{CC}=5.0V$	1.6		4.4	ns
Propagation delay from input ( $PRE$ or $CLR$ ) to output(Q or $\bar{Q}$ )	$t_{PLH}/t_{PHL}$	$V_{CC}=1.8V$	4.4		12.9	ns
		$V_{CC}=2.5V$	2.3		7	ns
		$V_{CC}=3.3V$	1.7		5.9	ns
		$V_{CC}=5.0V$	1.6		4.1	ns

■ OPERATING CHARACTERISTICS( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	$C_{PD}$	$f=10MHz$	$V_{CC}=1.8V$	35		pF
			$V_{CC}=2.5V$	35		pF
			$V_{CC}=3.3V$	37		pF
			$V_{CC}=5.0V$	40		pF

■ TEST CIRCUIT AND WAVEFORMS

From Output

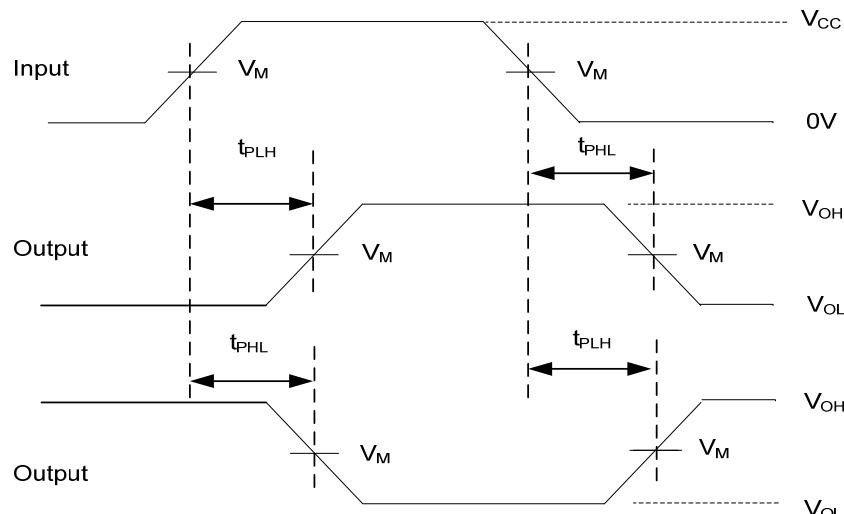


**TEST CIRCUIT**

Note:  $C_L$  includes probe and jig capacitance.

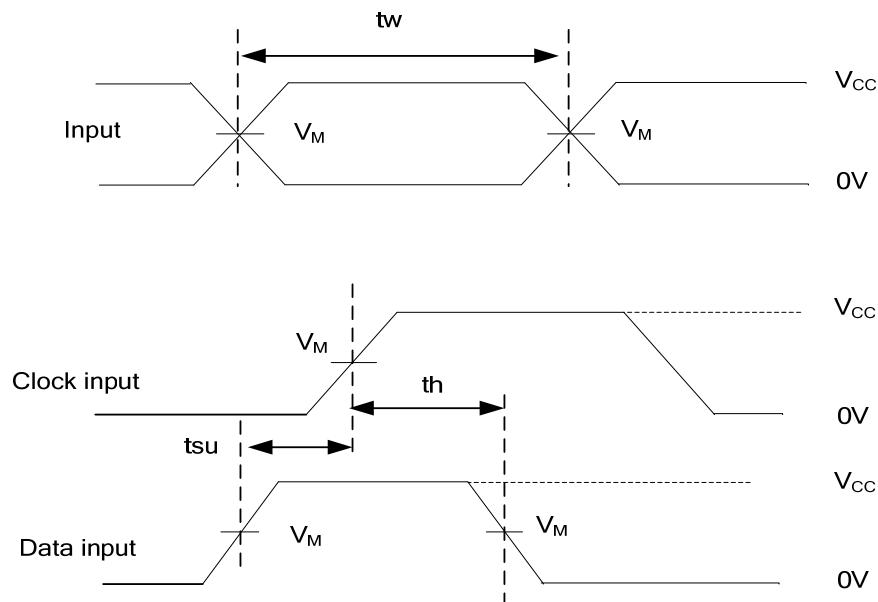
**Fig. 1 Load circuitry for switching times.**

$V_{CC}$	Inputs		$V_M$	$C_L$	$R_L$
	$V_{IN}$	$t_R, t_F$			
1.8V	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	$1\text{K}\Omega$
2.5V	$V_{CC}$	$\leq 2\text{ns}$	$V_{CC}/2$	30pF	$500\Omega$
3.3V	3V	$\leq 2.5\text{ns}$	1.5V	50pF	$500\Omega$
5V	$V_{CC}$	$\leq 2.5\text{ns}$	$V_{CC}/2$	50pF	$500\Omega$



**PROPAGATION DELAY TIMES**

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Note: All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10MHz,  $Z_0=50\Omega$

**Fig. 2 Propagation delay from input to output and input voltage waveforms.**

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