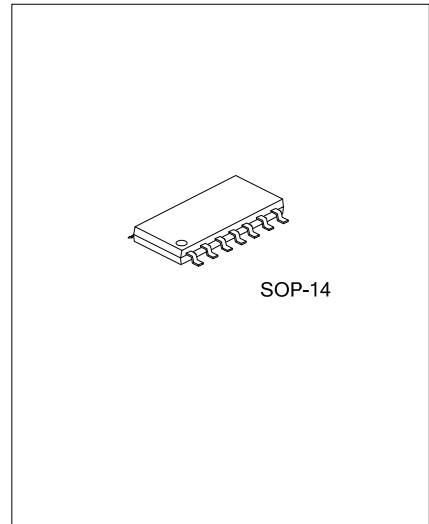




U74AC74

CMOS IC

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



DESCRIPTION

The **U74AC74** is a dual positive-edge-triggered D-type flip-flop. The preset (\overline{PRE}) and clear (\overline{CLR}) input can set or reset the output at a low level, regardless of the level of others inputs. When the \overline{PRE} and \overline{CLR} are inactive (high), data at the data D input meeting the set-up time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold-time interval, data D can be changed without affecting the levels at the outputs.

FEATURES

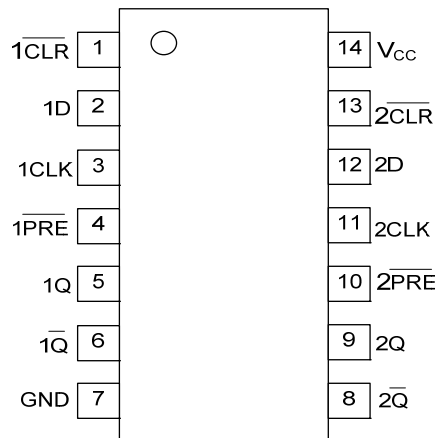
- * Operating voltage range: $V_{CC(OPR)}=2V$ to 6V.
- * Inputs accept voltages to 6V
- * Max tpd at 10ns of 5V

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AC74L-S14-R	U74AC74G-S14-R	SOP-14	Tape Reel

<p>U74AHC08G-S14-R</p> <p>(1) Packing Type (2) Package Type (3) Halogen Free</p>	<p>(1) R: Tape Reel (2) S14: SOP-14 (3) L: Lead Free, G: Halogen Free</p>
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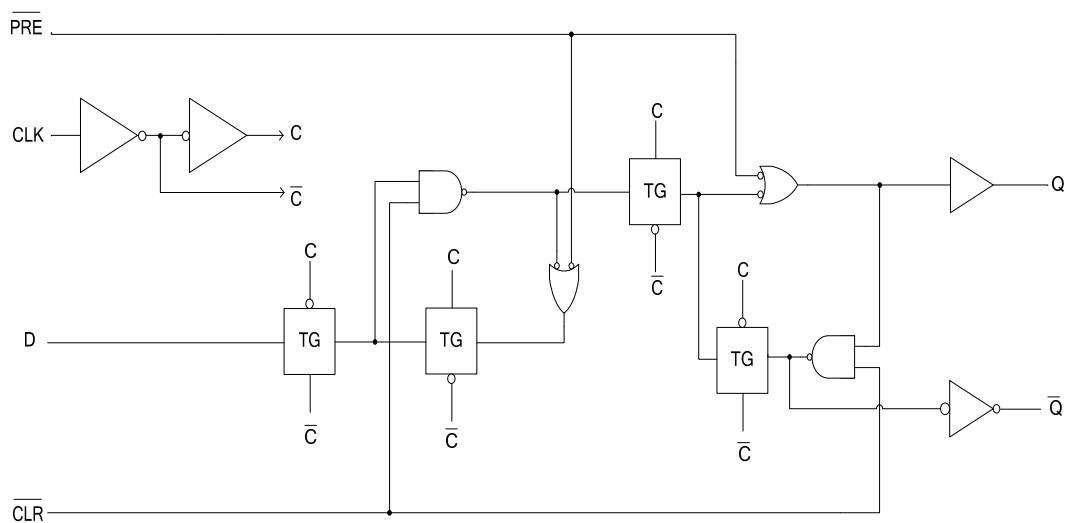
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT				OUTPUT	
PRE	CLR	CLK	D	Q	Q-bar
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q0

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5~7	V
Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
Output Voltage(active mode)	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Clamp Current(V _{IN} <0)	I _{IK}	-20(MIN)	mA
Output Clamp Current(V _{OUT} <0)	I _{OK}	±20	mA
Output Current	I _{OUT}	±50	mA
V _{CC} or GND Current	I _{CC}	±200	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		2		6	V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}		0		V _{CC}	V
High-level input voltage	V _{IH}	V _{CC} =3V	2.1			V
		V _{CC} =4.5V	3.15			
		V _{CC} =5.5V	3.85			
Low-level input voltage	V _{IL}	V _{CC} =3V			0.9	V
		V _{CC} =4.5V			1.35	
		V _{CC} =5.5V			1.65	
High-level Output Current	I _{OH}	V _{CC} =3V			-12	mA
		V _{CC} =4.5V			-24	
		V _{CC} =5.5V			-24	
Low-level Output Current	I _{OL}	V _{CC} =3V			12	mA
		V _{CC} =4.5V			24	
		V _{CC} =5.5V			24	
Input Transition Rise or Fall Rate	Δt/Δv				8	ns/V
Operating Temperature	T _A		-40		+85	°C

■ STATIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V _{OH}	I _{OH} =-50uA	V _{CC} =3V	2.9		V
			V _{CC} =4.5V	4.4		
			V _{CC} =5.5V	5.4		
		I _{OH} =-12mA	V _{CC} =3V	2.56		
			V _{CC} =4.5V	3.86		
			V _{CC} =5.5V	4.86		
Low-Level Output Voltage	V _{OL}	I _{OL} =-50uA	V _{CC} =3V		0.1	V
			V _{CC} =4.5V		0.1	
			V _{CC} =5.5V		0.1	
		I _{OL} =12mA	V _{CC} =3V		0.36	
			V _{CC} =4.5V		0.36	
			V _{CC} =5.5V		0.36	
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0V ~ 5.5V, V _{IN} =V _{CC} or GND			±0.1	μA
Quiescent Supply Current	I _{CC}	V _{CC} = 5.5V, V _{IN} =5.5V or GND I _{OUT} =0			2	
Input Capacitance	C _{IN}	V _{CC} =3.3V, V _{IN} =V _{CC} or GND		3		pF

■ DYNAMIC CHARACTERISTICS

T_A=25°C, unless otherwise specified, Input: t_R, t_F≤2.5ns; PRR≤1MHz

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency	F _{CLOCK}	V _{CC} =3V±0.3V			100	MHz
Pulse duration	tw	V _{CC} =3V±0.3V, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ in Low	5.5			ns
		V _{CC} =3V±0.3V, CLK	5.5			
Setup time before CLK↑	tsu	V _{CC} =3V±0.3V, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0			ns
		Data	4			
Hold time ,data after CLK↑	th	V _{CC} =3V±0.3V	0.5			ns
Clock frequency	F _{CLOCK}	V _{CC} =5V±0.5V			140	MHz
Pulse duration	tw	V _{CC} =5V±0.5V, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ in Low	4.5			ns
		V _{CC} =3V±0.3V, CLK	4.5			
Setup time before CLK↑	tsu	V _{CC} =5V±0.5V, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0			ns
		Data	3			
Hold time ,data after CLK↑	th	V _{CC} =5V±0.5V	0.5			ns

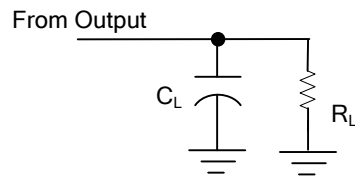
■ DYNAMIC CHARACTERISTICS (See Fig. 1 and Fig. 2 for test circuit and waveforms.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock	F _{MAX}	V _{CC} =3V±0.3V, C _L =50pF, R _L =500Ω	100	125		MHz
Propagation delay from input ($\overline{\text{PRE}}$ or $\overline{\text{CLR}}$) to output(Q or Q)	t _{PLH}	V _{CC} =3V±0.3V, C _L =50pF, R _L =500Ω	3.5	8	12	ns
	t _{PHL}		4	10.5	12	
Propagation delay from input (CLK) to output(Q or Q)	t _{PLH}	V _{CC} =3V±0.3V, C _L =50pF, R _L =500Ω	4.5	8	13.5	ns
	t _{PHL}		3.5	8	14	
Maximum clock	F _{MAX}	V _{CC} =5V±0.5V	140	160		MHz
Propagation delay from input ($\overline{\text{PRE}}$ or $\overline{\text{CLR}}$) to output(Q or Q)	t _{PLH}	V _{CC} =5V±0.5V, C _L =50pF, R _L =500Ω	2.5	6	9	ns
	t _{PHL}		3	8	9.5	
Propagation delay from input (CLK) to output(Q or Q)	t _{PLH}	V _{CC} =5V±0.5V, C _L =50pF, R _L =500Ω	3.5	6	10	ns
	t _{PHL}		2.5	6	10	

OPERATING CHARACTERISTICS

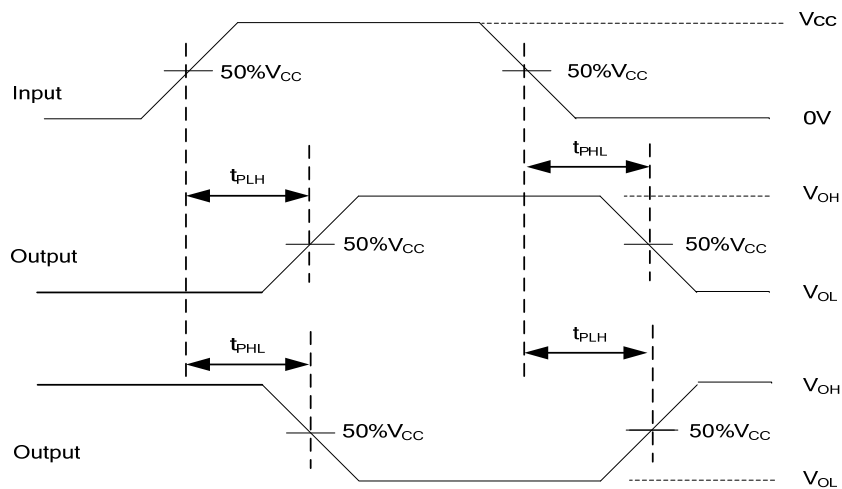
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	C _L =50p, f=1MHz, V _{CC} =3.3V		45		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

Note: C_L includes probe and jig capacitance.



PROPAGATION DELAY TIMES

Fig. 1 Load circuitry for switching times.

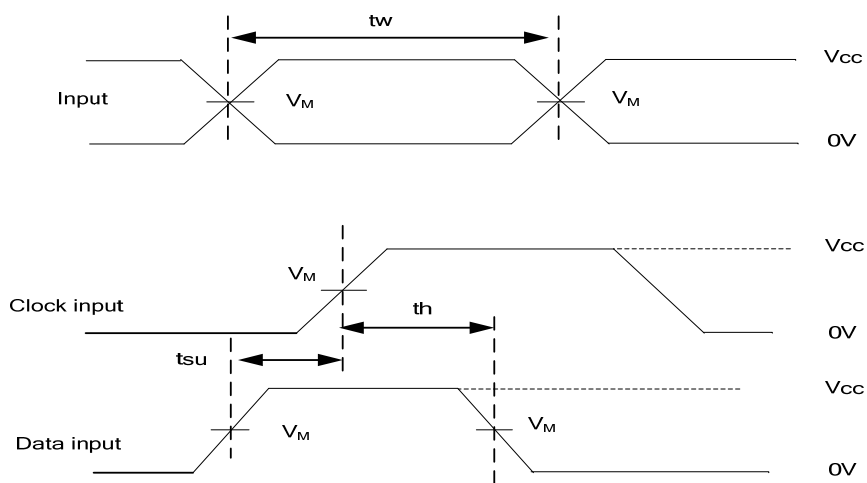


Fig. 2 Propagation delay from input to output and input voltage waveforms.

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