



U74HCT373

CMOS IC

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

DESCRIPTION

The **U74HCT373** is an octal transparent D-type latch with 3-state outputs, and it has 8 channels.

When the \overline{OE} input is low and the LE input is high, the Q outputs follow the D inputs. When \overline{OE} is low and LE is low, the Q outputs are latched at the logic levels of the D inputs.

When the \overline{OE} input is high, the outputs are in the high-impedance. The \overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

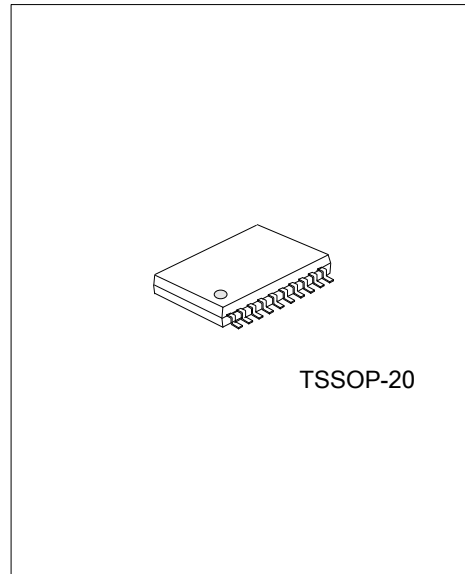
FEATURES

- * Inputs are TTL-Voltage Compatible
- * Operate from 4.5V to 5.5V
- * Inputs Accept Voltages to 5.5V
- * Max t_{PD} of 21ns at $V_{CC}=5.5V$, $C_L=50pF$
- * Typ $V_{OL} < 0.26V$ at $V_{CC}=4.5V$, $I_{OL}=6mA$, $T_A=25^\circ C$
- * Typ $V_{OH} > 3.94V$ at $V_{CC}=4.5V$, $I_{OH}=-6mA$, $T_A=25^\circ C$

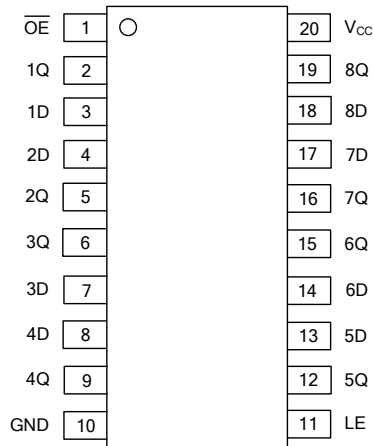
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT373L-P20-R	U74HCT373G-P20-R	TSSOP-20	Tape Reel
U74HCT373L-P20-T	U74HCT373G-P20-T	TSSOP-20	Tube

<p>U74HCT373L-P20-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) R: Tape Reel, T: Tube (2) P20: TSSOP-20 (3) G: Halogen Free, L: Lead Free</p>
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PIN CONFIGURATION

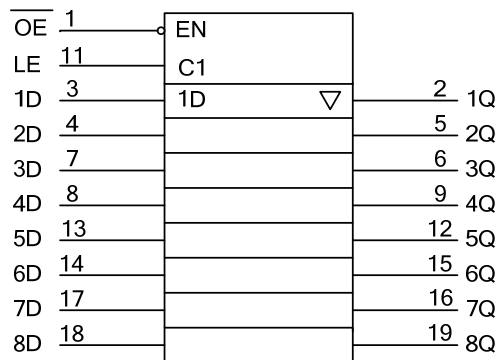


FUNCTION TABLE

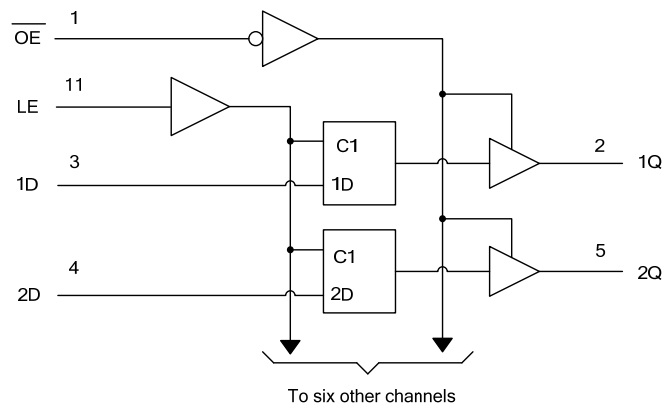
INPUTS(\overline{OE})	INPUTS(LE)	INPUTS(D)	OUTPUT(Q)
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Note: H: HIGH voltage level; L: LOW voltage level.

LOGIC SYMBOL



LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage	V_{CC}	-0.5 ~ 7	V
Input voltage (Note 3)	V_I	-0.5 ~ 7	V
Output voltage (Note 3)	V_O	-0.5 ~ $V_{CC} + 0.5$	V
Input clamp current	I_{IK}	-20	mA
Output clamp current	I_{OK}	±20	mA
Output current	I_O	±35	mA
V_{CC} or GND current	I_{CC}	±70	mA
Storage temperature	T_{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5		5.5	V
High-Level Input Voltage	V_{IH}	2			V
Low-Level Input Voltage	V_{IL}			0.8	V
Input Voltage	V_{IN}	0		5.5	V
Output Voltage	V_{OUT}	0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F			500	ns/V
Operating free-air temperature	T_A	-40		85	°C

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	$V_{CC}=4.5\text{V}, I_{OH}=-20\mu\text{A}$	4.4	4.499		V
		$V_{CC}=4.5\text{V}, I_{OH}=-6\text{mA}$	3.98	4.3		
Output Voltage Low-Level	V_{OL}	$V_{CC}=4.5\text{V}, I_{OL}=20\mu\text{A}$		0.001	0.1	V
		$V_{CC}=4.5\text{V}, I_{OL}=6\text{mA}$		0.17	0.26	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5\text{V}, V_{IN}=0$ or 5.5V		±0.1	±100	nA
Leakage Current (For Output in High-Impedance State)	I_{OZ}	$V_{CC}=5.5\text{V}, V_{IN}=V_{IH}$ or $V_{IH}, V_{OUT}=0$ or 5.5V		±0.01	±0.5	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5\text{V}, V_{IN}=V_{CC}$ or $\text{GND}, I_{OUT}=0$			8	μA
Additional quiescent supply current	ΔI_{CC}	$V_{CC}=5.5\text{V},$ one Input at 0.5V or $3.4\text{V},$ Other Inputs at V_{CC} or GND		1.4	2.4	mA
Input Capacitance	C_I	$V_{CC}=4.5\text{V}$ to 5V		3	10	pF

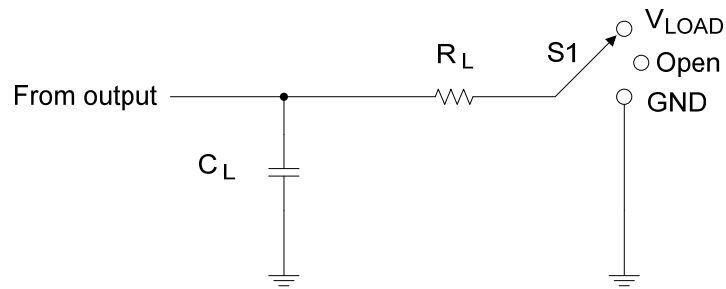
SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From D to Q	t_{PD} (t_{PLH}/t_{PHL})	$V_{CC}=4.5V, C_L=50pF$		25	35	ns
		$V_{CC}=5.5V, C_L=50pF$		21	32	
		$V_{CC}=4.5V, C_L=150pF$		32	52	
		$V_{CC}=5.5V, C_L=150pF$		27	47	
From LE to Q		$V_{CC}=4.5V, C_L=50pF$		28	35	
		$V_{CC}=5.5V, C_L=50pF$		25	32	
		$V_{CC}=4.5V, C_L=150pF$		38	52	
		$V_{CC}=5.5V, C_L=150pF$		36	47	
From \overline{OE} to Q	t_{EN} (t_{PZL}/t_{PZH})	$V_{CC}=4.5V, C_L=50pF$		26	35	ns
		$V_{CC}=5.5V, C_L=50pF$		23	32	
		$V_{CC}=4.5V, C_L=150pF$		33	52	
		$V_{CC}=5.5V, C_L=150pF$		28	47	
From \overline{OE} to Q	t_{DIS} (t_{PLZ}/t_{PHZ})	$V_{CC}=4.5V, C_L=50pF$		23	35	ns
		$V_{CC}=5.5V, C_L=50pF$		22	32	
Output transition rise/fall time	t_r (t_R/t_F)	$V_{CC}=4.5V, C_L=50pF$		10	12	ns
		$V_{CC}=5.5V, C_L=50pF$		9	11	
		$V_{CC}=4.5V, C_L=150pF$		18	42	
		$V_{CC}=5.5V, C_L=150pF$		16	38	
Pulse Width, LE high	t_w	$V_{CC}=4.5V$	20			ns
		$V_{CC}=5.5V$	17			
Setup Time, data before LE ↓	t_{SU}	$V_{CC}=4.5V$	10			ns
		$V_{CC}=5.5V$	9			
Hold Time, data after LE ↓	t_H	$V_{CC}=4.5V$	10			ns
		$V_{CC}=5.5V$	10			

OPERATING CHARACTERISTICS ($T_A=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	C_{PD}	No Load	50	pF

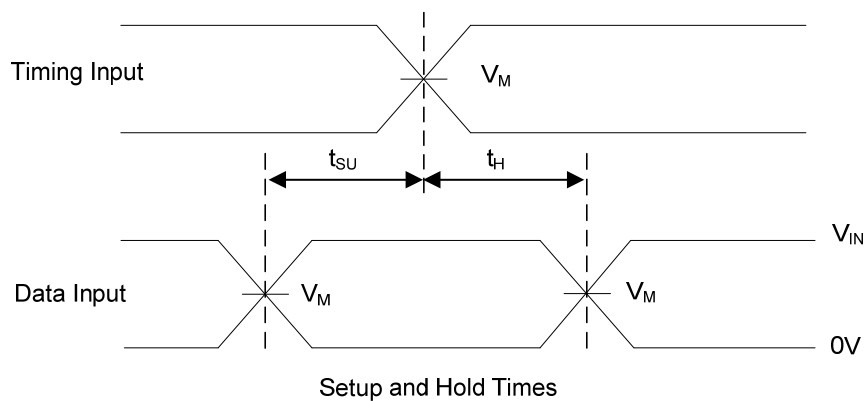
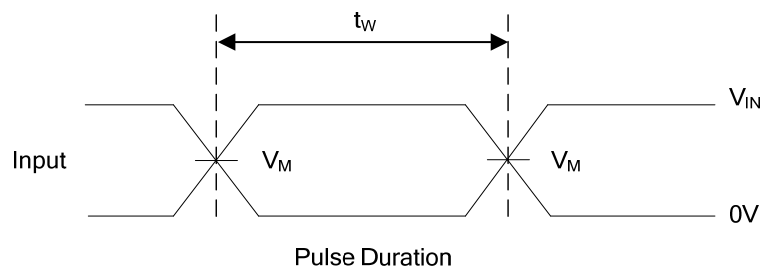
■ TEST CIRCUIT AND WAVEFORMS



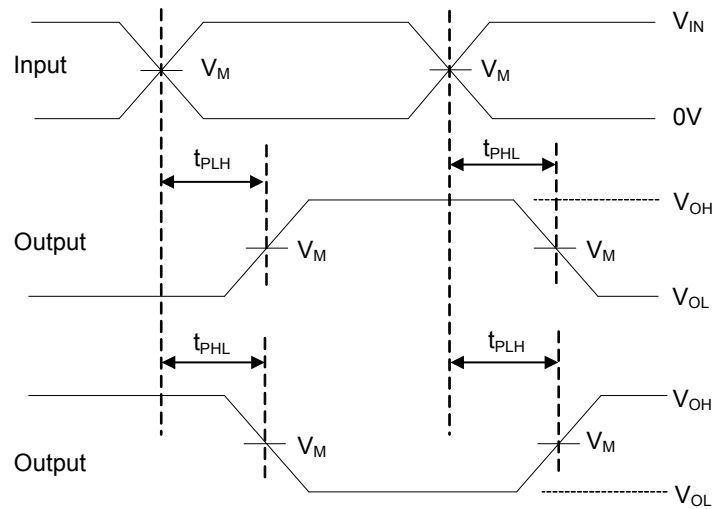
Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

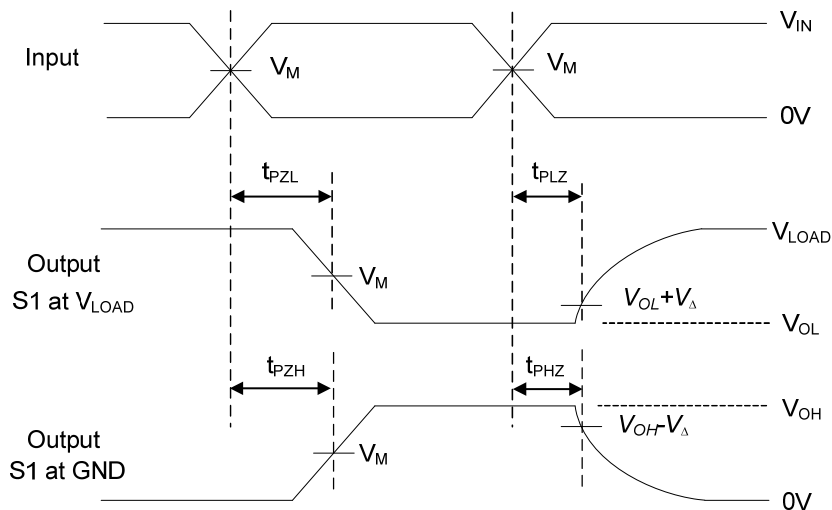
V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_{IN}	t_R, t_F					
$5V \pm 0.5V$	V_{CC}	$\leq 3ns$	$V_{CC}/2$	V_{CC}	15pF 50pF	1k Ω	0.5V



■ TEST CIRCUIT AND WAVEFORMS(Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Note: A. C_L includes probe and jig capacitance.

B. $P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 6\text{ns}$, $t_F \leq 6\text{ns}$.

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