

U74CBT3257C

CMOS IC

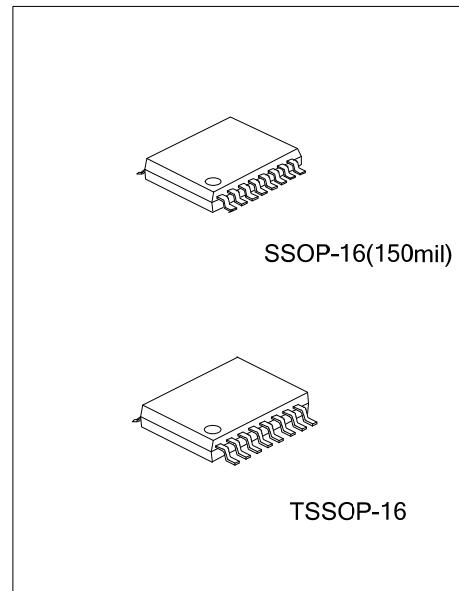
4-BIT 1-OF-2 FET MULTIPLEXER/ DEMULTIPLEXER

■ DESCRIPTION

The UTC U74CBT3257C is a 4-BIT 1-OF-2 FET multiplexer/demultiplexer with Low ON-State Resistance (R_{ON}) and TTL-compatibility.

■ FEATURES

- * Undershoot Protection for Off-Isolation on A and B Ports Up to -2V
- * V_{CC} Operating Range From 4V to 5.5V
- * Bidirectional Data Flow, With Near-Zero Propagation Delay
- * Low ON-State Resistance (R_{ON}) Characteristics ($R_{ON} = 3\Omega$ Typ.)
- * Low Power Consumption $I_{CC} = 3\mu A$ (Max)
- * Data and Control Inputs Provide Undershoot Clamp Diodes
- * Data I/Os Support 0 to 5-V Signaling Levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- * Control Inputs Can be Driven by TTL or 5V/3.3V CMOS Outputs
- * I_{OFF} Supports Partial-Power-Down Mode Operation
- * Supports I²C Bus Expansion



■ ORDERING INFORMATION

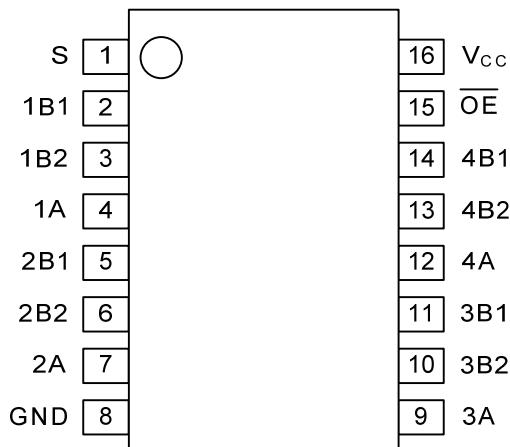
Ordering Number	Package	Packing
U74CBT3257CG-R16-R	SSOP-16	Tape Reel
U74CBT3257CG-P16-R	TSSOP-16	Tape Reel

U74CBT3257CG-R16-T	(1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) R16: SSOP-16, P16: TSSOP-16 (3) G: Halogen Free and Lead Free
--------------------	---	--

■ MARKING

SSOP-16	TSSOP-16
<p>SSOP-16 Pinout:</p> <ul style="list-style-type: none"> Pin 16, 15, 14, 13, 12, 11, 10, 9 are numbered at the top. A central box contains "UTC" above "CBT3257C". "Date Code" is indicated by a bracket pointing to the right. "Lot Code" is indicated by a bracket pointing to the right. Pin numbers 1 through 8 are listed at the bottom. 	<p>TSSOP-16 Pinout:</p> <ul style="list-style-type: none"> Pin 16, 15, 14, 13, 12, 11, 10, 9 are numbered at the top. A central box contains "UTC" above "CBT3257C". "Date Code" is indicated by a bracket pointing to the right. "Lot Code" is indicated by a bracket pointing to the right. Pin numbers 1 through 8 are listed at the bottom.

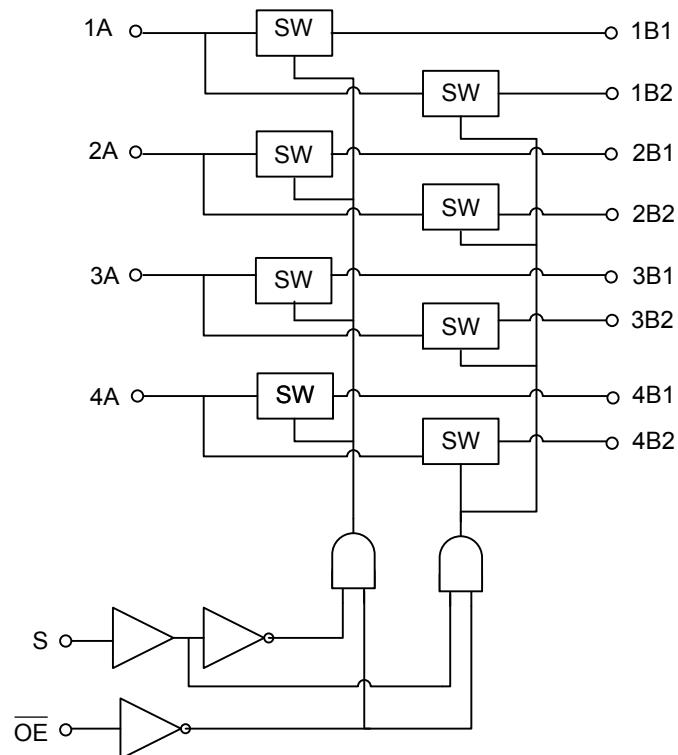
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUT		INPUT/OUTPUT A	FUNCTION
OE	S2		
L	L	B1	A port=B1 port
L	H	B2	A port=B2 port
H	X	Z	Disconnect

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
DC Input Voltage (Note 2, 3)	V_{IN}	-0.5 ~ 7	V
DC Switch Voltage (Note 2, 3)	$V_{IN(SW)}$	-0.5 ~ 7	V
	$V_{OUT(SW)}$		
Control Input Clamp Current	I_{IK}	-50	mA
DC V_{CC} or GND Current	I_{CC}	± 100	mA
ON-State Switch Current	$I_{IN(SW)}$	± 128	mA
	$I_{OUT(SW)}$		
Operating Temperature	T_{OPR}	-40~+85	$^\circ\text{C}$
Storage Temperature	T_{STG}	-65~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. All voltages are with respect to ground

3. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	90	$^\circ\text{C/W}$
		110	

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4		5.5	V
High-Level Control Input Voltage	V_{IH}	2		5.5	V
Low-Level Control Input Voltage	V_{IL}	0		0.8	V
Data Input Voltage	V_{IN}	0		5.5	V
Data Output Voltage	V_{OUT}	0		5.5	
Operating Temperature	T_A	-40		85	$^\circ\text{C}$

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

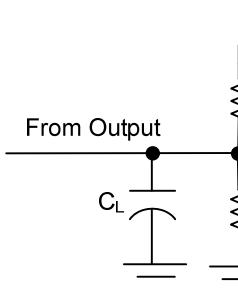
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Control Input Clamp Voltage	V_{IK}	$V_{CC}=4.5\text{V}$, $I_{IN} = -18\text{mA}$			-1.8	V
Data Inputs Clamp Voltage	V_{IKU}	$V_{CC}=5\text{V}$, $0\text{mA} > I_{IN} \geq -50\text{mA}$ GND, Switch OFF			-2	V
Input Leakage Current	$I_{(LEAK)}$	$V_{CC}=5.5\text{V}$, $V_{IN}=V_{CC}$ or GND			± 1	μA
Output OFF-State Current	I_{OZ}	$V_{CC}=5.5\text{V}$, $V_{OUT}=0$ to 5.5V , $V_{IN}=0$ $V_{IN}=V_{CC}$ or GND, Switch OFF			± 10	μA
Power OFF Leakage Current	I_{OFF}	$V_{CC}=0$, $V_O=0$ to 5.5V , $V_{IN}=0$			10	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5\text{V}$, $I_{IN}/I_{OUT}=0$ $V_{IN}=V_{CC}$ or GND, Switch ON or OFF			3	μA
Additional Quiescent Supply Current	ΔI_{CC}	$V_{CC}=5.5\text{V}$, One input at 3.4V , Other inputs at V_{CC} or GND			2.5	mA
Control Input Capacitance	C_{IN}	$V_{IN}=3\text{V}$ or 0 $V_{CC}=5\text{V}$		3.5		pF
A Port Input Capacitance	$C_{IO(OFF)}$	$V_{IN}/V_{OUT}=3\text{V}$ or 0, $V_{CC}=5\text{V}$		8.5		pF
B Port Input Capacitance		$V_{IN}=V_{CC}$ or GND, Switch OFF		5.5		pF
Port Input Capacitance	$C_{IO(ON)}$	$V_{I/O}=3\text{V}$ or 0, $V_{IN}=V_{CC}$ or 0, Switch ON		16.5		pF
ON-Resistance	R_{ON}	$V_{CC}=4\text{V}$, $V_{IN}=2.4\text{V}$, $I_{OUT}=-15\text{mA}$	8	12		Ω
		$V_{CC}=4.5\text{V}$, $V_{IN}=0$	$I_{OUT}=64\text{mA}$	3	6	Ω
			$I_{OUT}=30\text{mA}$	3	6	Ω
		$V_{CC}=4.5\text{V}$, $V_{IN}=2.4\text{V}$	$I_{OUT}=-15\text{mA}$	5	10	Ω

■ SWITCHING CHARACTERISTICS $C_L=50\text{pF}$ (see TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
From input (A or B) to output (B or A) (Note)	t_{PD}	$V_{CC}=4V, C_L=50\text{pF}, R_L=500\Omega$			0.24	ns	
		$V_{CC}=5V\pm0.5V, C_L=50\text{pF}, R_L=500\Omega$			0.15	ns	
From input S to output A	$t_{PD(S)}$	$V_{CC}=4V, C_L=50\text{pF}, R_L=500\Omega$			6.0	ns	
		$V_{CC}=5V\pm0.5V, C_L=50\text{pF}, R_L=500\Omega$	1.5		5.6	ns	
From input S to output B	t_{EN}	$V_{CC}=4V, C_L=50\text{pF}, R_L=500\Omega$			6.3	ns	
		$V_{CC}=5V\pm0.5V, C_L=50\text{pF}, R_L=500\Omega$	1.5		5.8	ns	
From input \overline{OE} to output (A or B)		$V_{CC}=4V, C_L=50\text{pF}, R_L=500\Omega$			6.3	ns	
		$V_{CC}=5V\pm0.5V, C_L=50\text{pF}, R_L=500\Omega$	1.5		5.8	ns	
From input S to output B	t_{DIS}	$V_{CC}=4V, C_L=50\text{pF}, R_L=500\Omega$			6.5	ns	
		$V_{CC}=5V\pm0.5V, C_L=50\text{pF}, R_L=500\Omega$	1.5		6.0	ns	
From input \overline{OE} to output (A or B)		$V_{CC}=4V, C_L=50\text{pF}, R_L=500\Omega$			5.9	ns	
		$V_{CC}=5V\pm0.5V, C_L=50\text{pF}, R_L=500\Omega$	1.5		5.9	ns	

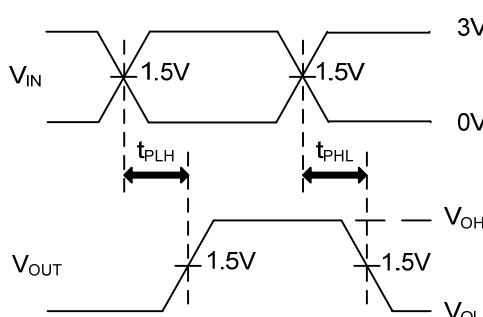
Note: The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

■ TEST CIRCUIT AND WAVEFORMS

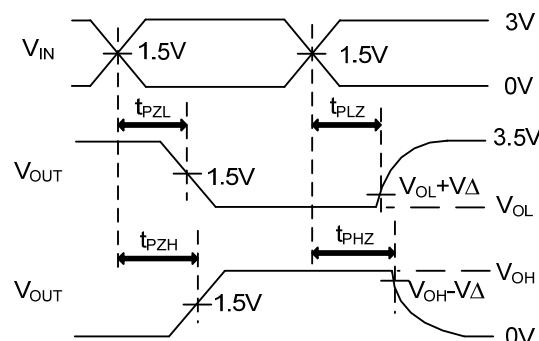


TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{EXT}

TEST	V_{CC}	V_I	t_R / t_F	V_Δ	S	C_L	R_L
t_{PLH}/t_{PHL}	4V	V_{CC} or GND	$\leq 2.5\text{ns}$		Open	50pF	500Ω
	$5V \pm 0.5V$	V_{CC} or GND	$\leq 2.5\text{ns}$		Open	50pF	500Ω
t_{PLZ}/t_{PZL}	4V	GND	$\leq 2.5\text{ns}$	0.3V	V_{EXT}	50pF	500Ω
	$5V \pm 0.5V$	GND	$\leq 2.5\text{ns}$	0.3V	V_{EXT}	50pF	500Ω
t_{PHZ}/t_{PZH}	4V	V_{CC}	$\leq 2.5\text{ns}$	0.3V	Open	50pF	500Ω
	$5V \pm 0.5V$	V_{CC}	$\leq 2.5\text{ns}$	0.3V	Open	50pF	500Ω



Propagation Delay Times



Enable and Disable Times

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 10\text{MHz}$, $Z_0 = 50\Omega$, $t_R \leq 2.5\text{ns}$, $t_F \leq 2.5\text{ ns}$.

3. The outputs are measured one at a time with one transition per measurement.

4. t_{PLZ} and t_{PHZ} are the same as t_{DIS} .

5. t_{PZL} and t_{PZH} are the same as t_{EN} .

6. t_{PLH} and t_{PHL} are the same as $t_{PD(S)}$.

7. All parameters and waveforms are not applicable to all devices.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.