UNISONIC TECHNOLOGIES CO., LTD

U74AHCT374

CMOS IC

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

TSSOP-20

■ DESCRIPTION

The **U74AHCT374** is a octal edge-triggered D-type flip-flops with 3-state outputs and 8 channels.

When the $\overline{OE}$ input is low, on the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

When the $\overline{OE}$ input is high, the outputs are in the high-impedance.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* Inputs are TTL-Voltage Compatible
* Operate from 4.5V to 5.5V
* Inputs Accept Voltages to 5.5V
* Max t_{PD} of 9.4ns at V_{CC}=5V, C_L=15pF
* Typical V_{OL}< 0.36V at V_{CC}=4.5V, I_{OL}=8mA, T_A=25°C
* Typical V_{OH}> 3.94V at V_{CC}=4.5V, I_{OH}=-8mA, T_A=25°C

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT374L-P20-R	U74AHCT374G-P20-R	TSSOP-20	Tape Reel
U74AHCT374L-P20-T	U74AHCT374G-P20-T	TSSOP-20	Tube

U74AHCT374L-P20-R

- (1)Packing Type
- (2)Package Type
- (3)Lead Free

(1) R: Tape Reel, T: Tube

(2) P20: TSSOP-20

(3) G: Halogen Free, L: Lead Free

U74AHCT374

■ **PIN CONFIGURATION**

$\overline{OE}$	1	20	V_{CC}
1Q	2	19	8Q
1D	3	18	8D
2D	4	17	7D
2Q	5	16	7Q
3Q	6	15	6Q
3D	7	14	6D
4D	8	13	5D
4Q	9	12	5Q
GND	10	11	CLK
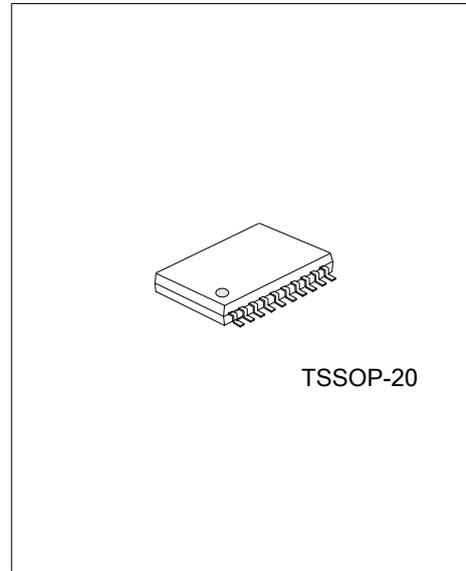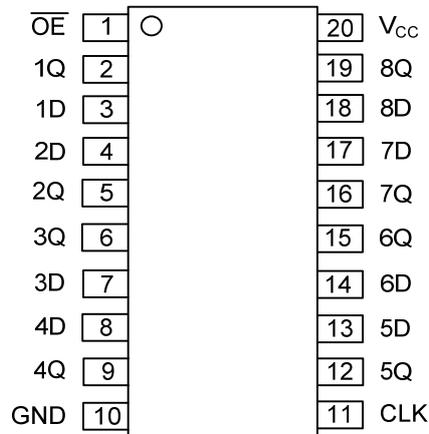
■ **FUNCTION TABLE**

INPUTS($\overline{OE}$)	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

■ **LOGIC SYMBOL**

■ **LOGIC DIAGRAM**

To six other channels

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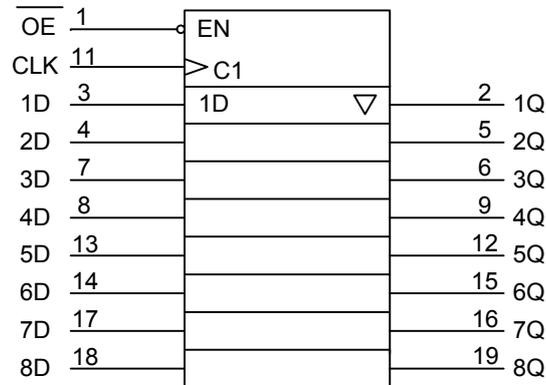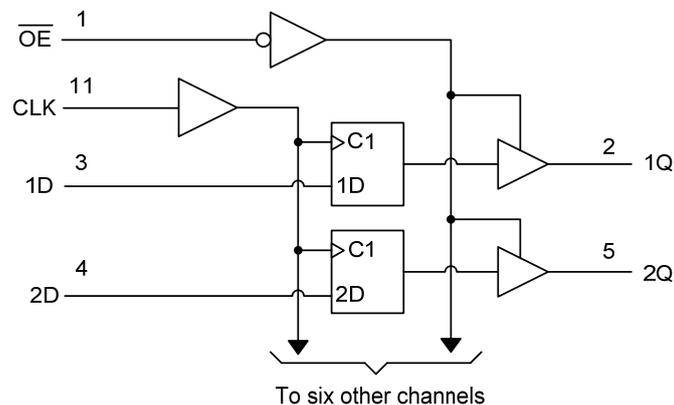
■ **ABSOLUTE MAXIMUM RATING**

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Voltage	V_{IN}	-0.5 ~ 7	V
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5	V
V_{CC} or GND Current	I_{CC}	±70	mA
Output Current	I_{OUT}	±35	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Operating Temperature	T_{OPR}	-40 ~ + 85	℃
Storage Temperature	T_{STG}	-65 ~ + 150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5		5.5	V
High-level Input Voltage	V_{IH}	2			V
Low-level Input Voltage	V_{IL}			0.8	V
Input Voltage	V_{IN}	0		5.5	V
Output Voltage	V_{OUT}	0		V_{CC}	V
High-Level Output Current	I_{OH}			-8	mA
Low-Level Output Current	I_{OL}			8	mA
Input Rise or Fall Times	t_R, t_F			20	ns/V
Operating free-Air Temperature	T_A	-40		85	℃

■ **ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	V_{CC}=4.5V, I_{OH}=-50µA	4.4	4.5		V
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			
Output Voltage Low-Level	V_{OL}	V_{CC}=4.5V, I_{OL}=50µA			0.1	V
		V_{CC}=4.5V, I_{OL}=8mA			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V to 5.5V, V_{IN}=0 or 5.5V			±0.1	µA
Leakage Current (For Output in High-Impedance State)	I_{OZ}	V_{CC}=5.5V,V_{IN}=V_{IH} or V_{IH},V_{OUT}=0 or 5.5V			±0.25	µA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	µA
Additional Quiescent Supply Current	$\triangle I_{CC}$	V_{CC}=5.5V, one input at 3.4V, Other inputs at V_{CC} or GND			1.35	mA
Input Capacitance	C_I	V_{CC}=5V, V_{IN}=V_{CC} or GND		4	10	pF
Output Capacitance	C_O	V_{CC}=5V, V_{OUT}=V_{CC} or GND		9		pF

■ **SWITCHING CHARACTERISTICS** (T_A =25℃, See TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
From CLK to Q	t_{PLH}/t_{PHL}	V_{CC} = 5 V ± 0.5 V	C_L =15pF		5.6	9.4	ns
			C_L =50pF		6.4	10.4	
From $\overline{OE}$ to Q	t_{PZL}/t_{PZH}	V_{CC} = 5 V ± 0.5 V	C_L =15pF		6.5	10.2	ns
			C_L =50pF		7.3	11.2	
From $\overline{OE}$ to Q	t_{PLZ}/t_{PHZ}	V_{CC} = 5 V ± 0.5 V	C_L =15pF		6.2	10.2	ns
			C_L =50pF		7	11.2	
Maximum Clock Frequency	f_{MAX}	V_{CC} = 5 V ± 0.5 V	C_L =15pF		90	140	MHz
			C_L =50pF		85	130	
Pulse Width	t_W	V_{CC} = 5 V ± 0.5 V			6.5		ns
Setup Time	t_{SU}	V_{CC} = 5 V ± 0.5 V			2.5		ns
Hold Time	t_H	V_{CC} = 5 V ± 0.5 V			2.5		ns

■ **OPERATING CHARACTERISTICS**(T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load, V_{CC} = 5 V, f=1MHz		27		pF

■ **TEST CIRCUIT AND WAVEFORMS**
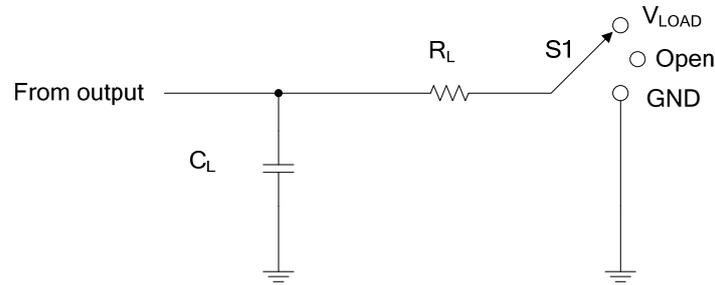
Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
5V±0.5V	V_{CC}	≤3ns	$V_{CC}/2$	V_{CC}	15pF	1kΩ	0.5V
					50pF		

Pulse Duration

Setup and Hold Times
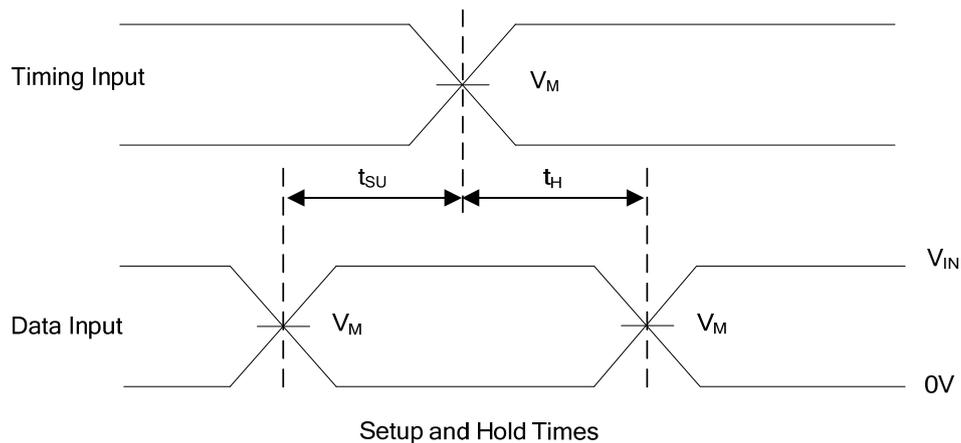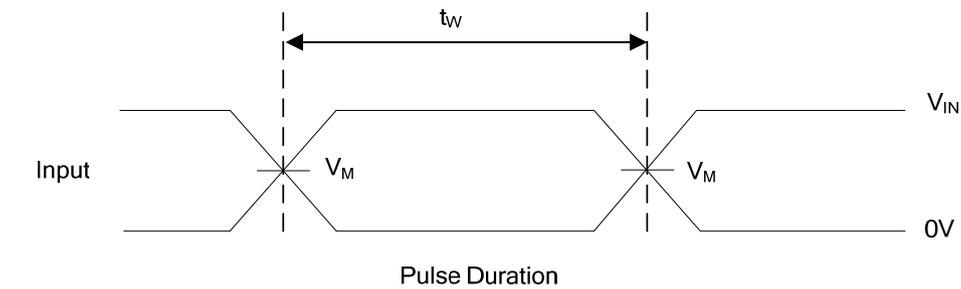
■ **TEST CIRCUIT AND WAVEFORMS(Cont.)**
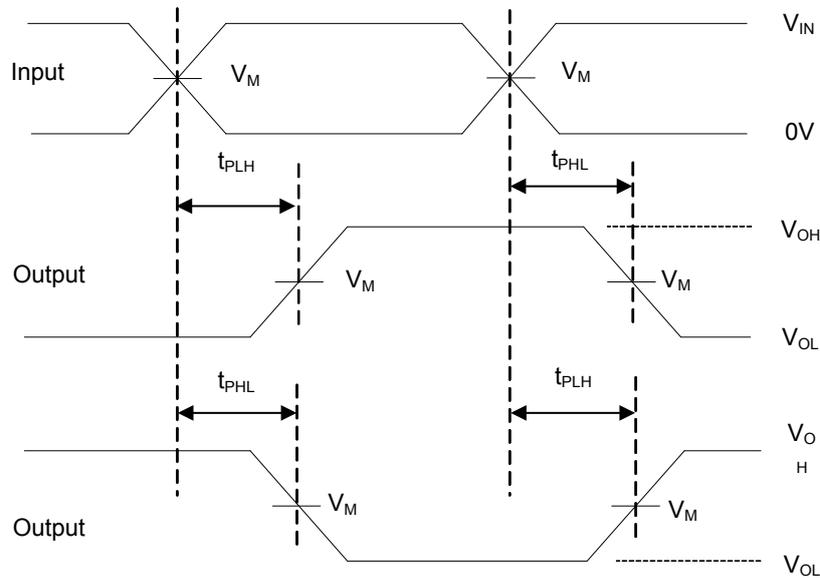
Voltage Waveforms Propagation Delay Times
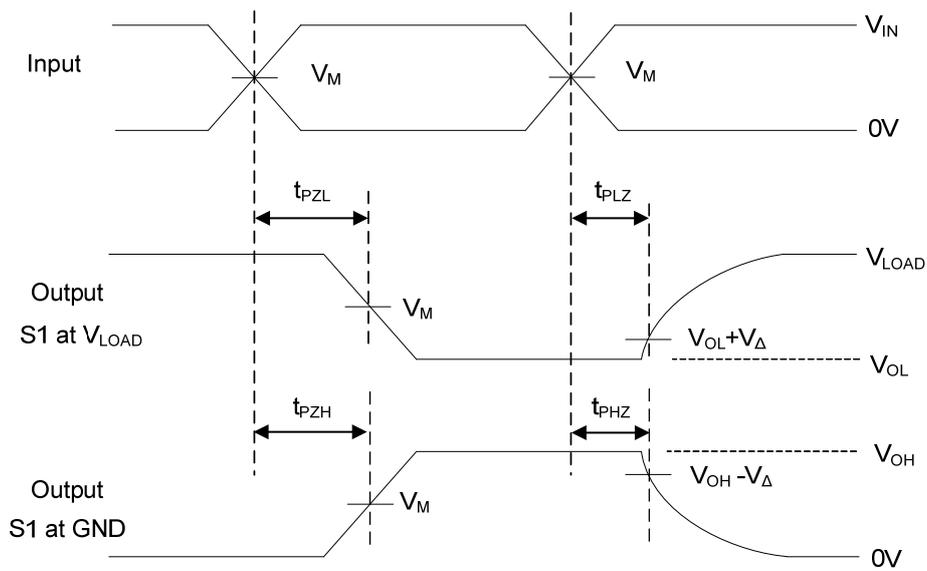
Voltage Waveforms Enable and Disable Times

Note: A. C_L includes probe and jig capacitance.

      B. $P_{RR} \leqslant 1MHz$, $Z_O = 50\Omega$, $t_R \leqslant 3ns$, $t_F \leqslant 3ns$.