



U74AHC3G04

CMOS IC

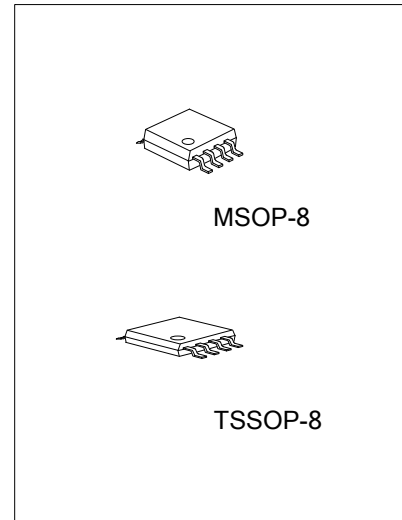
INVERTER

DESCRIPTION

The **U74AHC3G04** are high-speed Si-gate CMOS devices providing three inverting buffers with the function $Y = \overline{A}$.

FEATURES

- * Low Power Dissipation
- * Symmetrical Output Impedance
- * Balanced Propagation Delays
- * High Noise Immunity



ORDERING INFORMATION

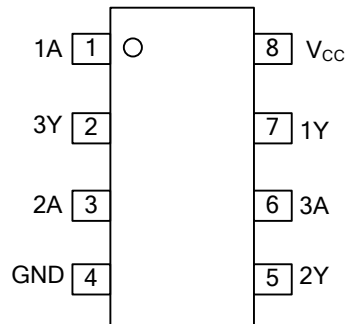
Ordering Number	Package	Packing
U74AHC3G04G-SM1-R	MSOP-8	Tape Reel
U74AHC3G04G-P08-R	TSSOP-8	Tape Reel

<p>U74AHC3G04G-P08-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) P08: TSSOP-8, SM1:MSOP-8 (3) G: Halogen Free and Lead Free</p>
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MARKING

MSOP-8	TSSOP-8
<p>UTC □□□□ → Date Code AHC3G04G □□ → Lot Code</p>	<p>UTC □□□□ → Date Code AHC3G04G □□ → Lot Code</p>

■ PIN CONFIGURATION



For TSSOP-8, MSOP-8

■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(Y)
L	H
H	L

■ LOGIC DIAGRAM (each gate)



■ ABSOLUTE MAXIMUM RATING (T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 7.0	V
Input Voltage	V _{IN}	-0.5 ~ 7.0	V
Output Voltage	V _{OUT}	-0.5 ~ V _{CC} +0.5	V
V _{CC} or GND Current	I _{CC}	±75	mA
Output Current	I _{OUT}	±25	mA
Input Clamp Current	I _{IK}	-20	mA
Output Clamp Current	I _{OK}	±20	mA
Operating Temperature	T _{OPR}	-40 ~ + 85	°C
Storage Temperature	T _{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		2.0	5.0	5.5	V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}		0		V _{CC}	V
Input Rise or Fall Times	t _R , t _F	V _{CC} = 3.3 ± 0.3V			100	ns/V
		V _{CC} = 5.0 ± 0.5V			20	

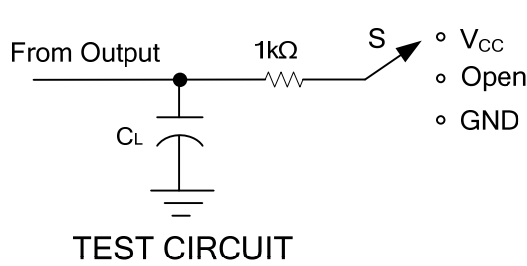
■ ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	UNIT
High-Level input voltage	V _{IH}		2.0	1.5			V
			3.0	2.1			
			5.5	3.85			
Low-Level input voltage	V _{IL}		2.0			0.5	V
			3.0			0.9	
			5.5			1.65	
High-Level Output Voltage	V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -50μA	2.0	1.9	2.0		V
		V _I = V _{IH} or V _{IL} , I _{OH} = -50μA	3.0	2.9	3.0		
		V _I = V _{IH} or V _{IL} , I _{OH} = -50μA	4.5	4.4	4.5		
		V _I = V _{IH} or V _{IL} , I _{OH} = -4.0mA	3.0	2.58			
		V _I = V _{IH} or V _{IL} , I _{OH} = -8.0mA	4.5	3.94			
Low-Level Output Voltage	V _{OL}	V _I = V _{IH} or V _{IL} , I _{OH} = 50μA	2.0			0.1	V
		V _I = V _{IH} or V _{IL} , I _{OH} = 50μA	3.0			0.1	
		V _I = V _{IH} or V _{IL} , I _{OH} = 50μA	4.5			0.1	
		V _I = V _{IH} or V _{IL} , I _{OH} = 4.0mA	3.0			0.36	
		V _I = V _{IH} or V _{IL} , I _{OH} = 8.0mA	4.5			0.36	
Input Leakage Current	I _{I(LEAK)}	V _{IN} =V _{CC} or GND	5.5			0.1	μA
Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND, I _{OUT} =0	5.5			10	μA
Input Capacitance	C _{IN}	V _{IN} =V _{CC} or GND			1.5	10	pF

■ SWITCHING CHARACTERISTICS ($t_R = t_F \leq 3.0$ ns, $T_A = 25^\circ\text{C}$)

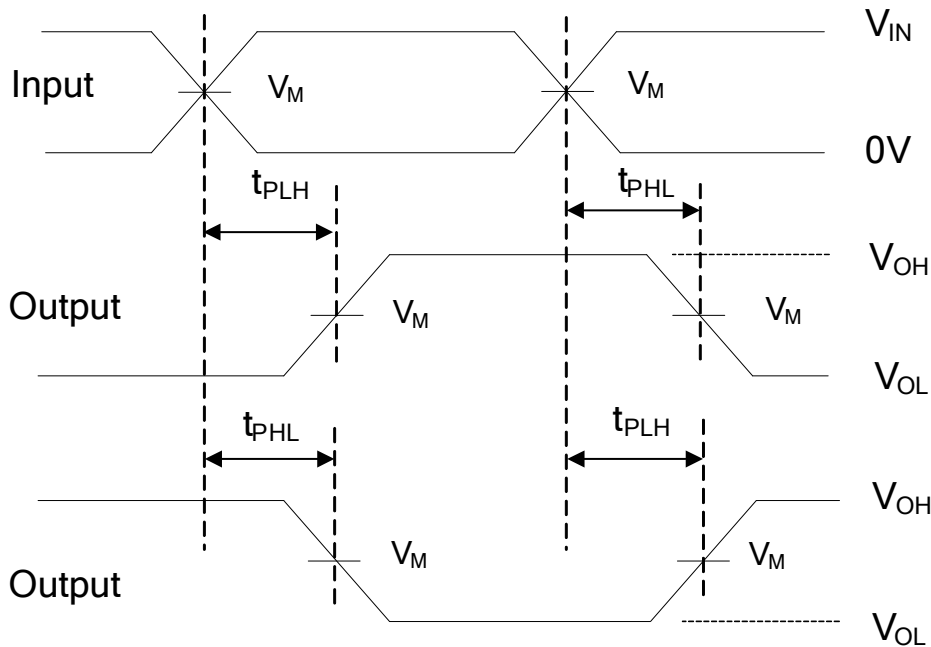
PARAMETER	SYMBOL	C_L (pF)	V_{CC} (V)	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH} t_{PHL}	15	3.0 to 3.6			7.1	ns
			3.3		4.3		
			4.5 to 5.5			5.5	
			5		3.1		
		50	3.0 to 3.6			10.6	ns
			3.3		6.1		
			4.5 to 5.5			7.5	
			5		4.5	-	

■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}

V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
GND to V_{CC}	$50\%V_{CC}$	$50\%V_{CC}$



Propagation delay times
Inverting and noninverting outputs

Note: C_L includes probe and jig capacitance.
 $P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 3\text{ns}$, $t_F \leq 3\text{ns}$.

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