

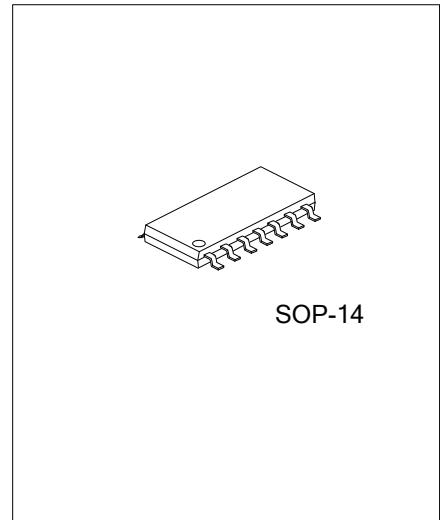


UCD4011B

Preliminary

CMOS IC

QUAD 2-INPUT NAND BUFFERED B SERIES GATE



DESCRIPTION

The **UTC UCD4011B** contains four independent 2-input NAND gates which perform the function $Y = \overline{A \bullet B}$ in positive logic.

FEATURES

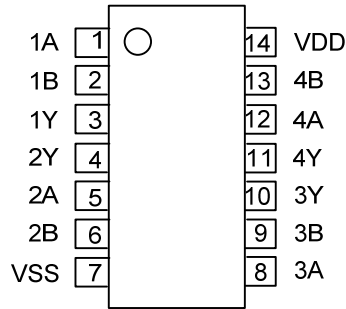
- * 5V-10V-15V Parametric Ratings
- * Quad 2-Input NAND Gate
- * Symmetrical Output Characteristics
- * Maximum Input Current of 1uA at 15V Over Full Package Temperature Range
- * Low Power TTL:
Fan Out of 2 Driving 74L or 1 Driving 74LS Compatibility

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4011BL-S14-R	UCD4011BG-S14-R	SOP-14	Tape Reel

<p>UCD4011BL-S14-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Lead Plating 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S14: SOP-14 (3) L: Lead Free, G: Halogen Free
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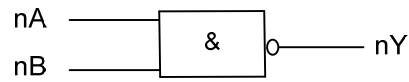
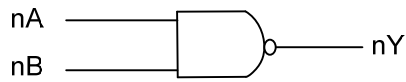
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	L
H	L	H
L	H	H
L	L	H

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5 ~ 18	V
Input Voltage	$V(nA, nB)$	-0.5 ~ $V_{DD} + 0.5$	V
Output Voltage	$V(nY)$	-0.5 ~ $V_{DD} + 0.5$	V
Storage Temperature	T_{STG}	-65 ~ + 150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	3 ~ 15	V
Operating Temperature	T_{OP}	-55 ~ 125	$^\circ\text{C}$

■ ELECTRICAL CHARACTERISTICS($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{DD}= 5V, V_O=0.5V$	3.5	3		V
		$V_{DD}= 10V, V_O=1.0V$	7.0	6		
		$V_{DD}= 15V, V_O=1.5V$	11.0	9		
Low-Level Input Voltage	V_{IL}	$V_{DD}= 5V, V_O=4.5V$		2	1.5	V
		$V_{DD}= 10V, V_O=9.0V$		4	3.0	
		$V_{DD}= 15V, V_O=13.5V$		6	4.0	
High-Level Output Voltage	V_{OH}	$V_{DD}= 5V, I_O < 1\mu A$	4.95	5		V
		$V_{DD}= 10V, I_O < 1\mu A$	9.95	10		
		$V_{DD}= 15V, I_O < 1\mu A$	14.95	15		
Low-Level Output Voltage	V_{OL}	$V_{DD}= 5V, I_O < 1\mu A$		0	0.05	V
		$V_{DD}= 10V, I_O < 1\mu A$		0	0.05	
		$V_{DD}= 15V, I_O < 1\mu A$		0	0.05	
High-Level Output Current (NOTE)	I_{OH}	$V_{DD}= 5V, V_O=4.6V$	-0.51	-0.88		mA
		$V_{DD}= 10V, V_O=9.5V$	-1.3	-2.25		
		$V_{DD}= 15V, V_O=13.5V$	-3.4	-8.8		
Low-Level Output Current (NOTE)	I_{OL}	$V_{DD}= 5V, V_O=0.4V$	0.51	0.88		mA
		$V_{DD}= 10V, V_O=0.5V$	1.3	2.25		
		$V_{DD}= 15V, V_O=1.5V$	3.4	8.8		
Input Leakage Current	$I_{I(LEAK)}$	$V_{DD}= 15V, V_{IN} = V_{DD}$ or GND			0.1	μA
Quiescent Supply Current	I_Q	$V_{DD}= 5V, V_{IN} = V_{DD}$ or VSS, $I_{OUT} = 0$		0.004	0.25	μA
		$V_{DD}= 10V, V_{IN} = V_{DD}$ or VSS, $I_{OUT} = 0$		0.005	0.5	
		$V_{DD}= 15V, V_{IN} = V_{DD}$ or VSS, $I_{OUT} = 0$		0.006	1.0	

Note: I_{OL} and I_{OH} are tested one output at a time

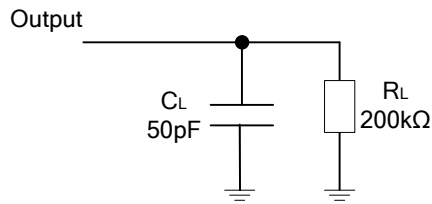
■ SWITCHING CHARACTERISTICS($T_A=25^\circ\text{C}$, Input: $t_R=t_F=20\text{ns}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	$V_{DD}=5\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		85	250	ns
		$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	100	
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		30	70	
	t_{PHL}	$V_{DD}=5\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		120	250	
		$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		50	100	
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		35	70	
Transition Time	t_{TLH} t_{THL}	$V_{DD}=5\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		90	200	ns
		$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		50	100	
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	80	

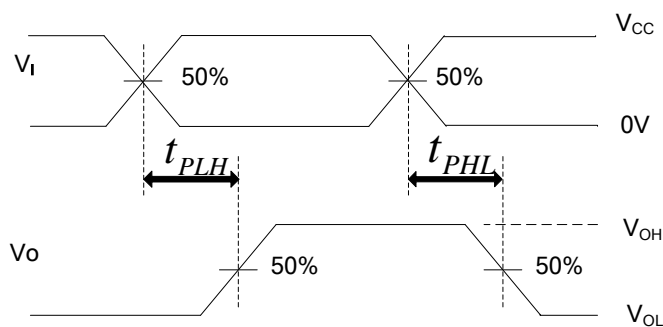
■ OPERATING CHARACTERISTICS($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF
Power Dissipation Capacitance	C_{pd}	Any Gate		14		

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit



Propagation Delay Times

Note: C_L includes probe and jig capacitance.

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