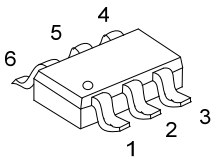
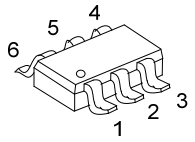
U74LVC2G04

CMOS IC

DUAL INVERTER



SOT-26



SOT-363

■ DESCRIPTION

The **U74LVC2G04** is a dual inverter gate and it provides the Boolean function $Y=\overline{A}$ in positive logic.

This device has power-down protective circuit to prevent the device from destruction when it is powered down.

■ FEATURES

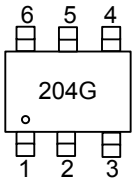
* Operate From 1.65V To 5.5V
* Inputs Accept Voltages To 5.5V
* High Noise Immunity
* Low Power Dissipation
* Max t_{PD} Of 3.2 ns At 5V

■ ORDERING INFORMATION

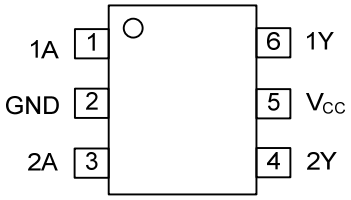
Ordering Number	Package	Packing
U74LVC2G04G-AG6-R	SOT-26	Tape Reel
U74LVC2G04G-AL6-R	SOT-363	Tape Reel

U74LVC2G04G-AG6-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AG6: SOT-26, AL6: SOT-363 (3) G: Halogen Free and Lead Free

■ MARKING



■ PIN CONFIGURATION

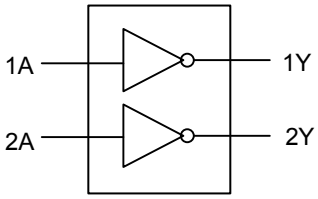


■ FUNCTION TABLE

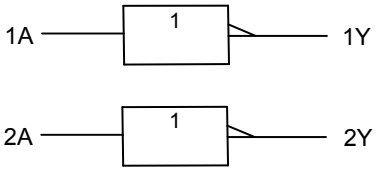
INPUT(nA)	OUTPUT(nY)
H	L
L	H

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Active Mode	V_{OUT}	-0.5 ~ V_{CC} +0.5	V
	Power-Down Mode		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Continuous Output Current (V_{OUT}=0 to V_{CC})		I_{OUT}	±50	mA
Input Clamp Current (V_{IN}<0)		I_{IK}	-50	mA
Output Clamp Current (V_{OUT}>V_{CC} or V_{OUT}<0)		I_{OK}	±50	mA
Power Dissipation (T_A=-40°C ~ +125°C)		P_D	300	mW
Operating Junction Temperature		T_J	-40 ~ +125	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	1.65		5.5	V
Input Voltage		V_{IN}	0		5.5	V
Output Voltage	Active Mode	V_{OUT}	0		V_{CC}	V
	Power-Down Mode		0		5.5	V
Input Transition Rise or Fall Rate	V_{CC}=1.65V to 2.7V	t_R / t_F	0		20	ns/V
	V_{CC}=2.7V to 5.5V		0		10	ns/V

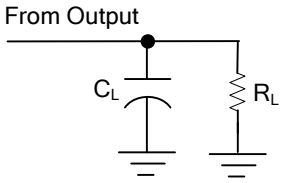
■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=1.65V ~ 1.95V	0.65×V_{CC}			V
		V_{CC}=2.3V ~ 2.7V	1.7			V
		V_{CC}=2.7V ~ 3.6V	2			V
		V_{CC}=4.5V ~ 5.5V	0.7×V_{CC}			V
Low-level Input Voltage	V_{IL}	V_{CC}=1.65V ~ 1.95V			0.35×V_{CC}	V
		V_{CC}=2.3V ~ 2.7V			0.7	V
		V_{CC}=2.7V ~ 3.6V			0.8	V
		V_{CC}=4.5V ~ 5.5V			0.3×V_{CC}	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65 ~ 5.5V, I_{OH}=-100μA	V_{CC}-0.1			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9			V
		V_{CC}=2.7V, I_{OH}=-12mA	2.2			V
		V_{CC}=3.0V, I_{OH}=-24mA	2.3			V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65 ~ 5.5V, I_{OL}=100μA			0.1	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45	V
		V_{CC}=2.3V, I_{OL}=8mA			0.3	V
		V_{CC}=2.7V, I_{OL}=12mA			0.4	V
		V_{CC}=3.0V, I_{OL}=24mA			0.55	V
		V_{CC}=4.5V, I_{OL}=32mA			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=5.5V or GND		±0.1	±5	μA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=5.5V		±0.1	±10	μA
Quiescent Supply Current	I_Q	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0		0.1	10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=2.3 ~ 5.5V, One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND		5	500	μA

■ SWITCHING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

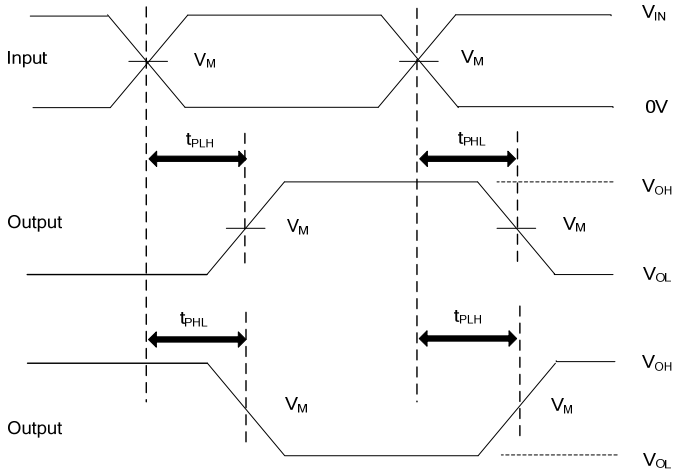
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH} t_{PHL}	C_L=30pF	V_{CC}=1.8±0.15V, R_L=1KΩ	1.0	3.5	8.0	ns
			V_{CC}=2.5±0.2V, R_L=500Ω	1.0	2.2	4.4	ns
		C_L=50pF	V_{CC}=2.7V, R_L=500Ω	1.0	2.7	5.2	ns
			V_{CC}=3.3±0.3V, R_L=500Ω	0.5	2.7	4.1	ns
			V_{CC}=5±0.5V, R_L=500Ω	1.0	1.9	3.2	ns

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	Inputs		V_M	C_L	R_L
	V_{IN}	t_R, t_F			
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	30pF	1KΩ
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	30pF	500Ω
2.7V	2.7V	≤2.5ns	1.5V	50pF	500Ω
3.3V±0.3V	2.7V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	50pF	500Ω



PROPAGATION DELAY TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O=50Ω.