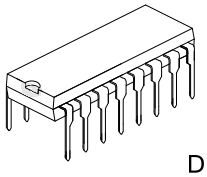
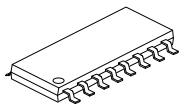
U74HC595A

CMOS IC

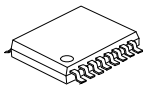
8-BIT SERIAL-IN SHIFT REGISTER WITH LATCHED 3-STATE PARALLEL OUTPUTS, PROVIDING SERIAL OUTPUT



DIP-16



SOP-16



TSSOP-16

■ DESCRIPTION

The UTC **74HC595A** contains an 8-bit register with asynchronous reset input and an 8-bit latch with output. The Serial Data Input (A) will shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

■ FEATURES

* Operation Voltage Range:2~6V
* High Noise Immunity
* Output Compatibility with CMOS and TTL
* Specified from -40~+125°C

■ ORDERING INFORMATION

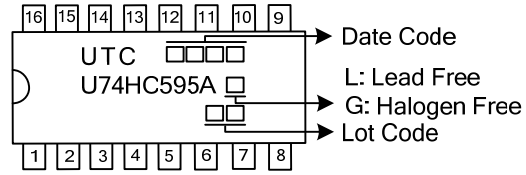
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC595AL-D16-T	U74HC595AG-D16-T	DIP-16	Tube
-	U74HC595AG-S16-R	SOP-16	Tape Reel
-	U74HC595AG-P16-R	TSSOP-16	Tape Reel

U74HC595AL-D16-T
(1)Packing Type
(2)Package Type
(3)Green Package

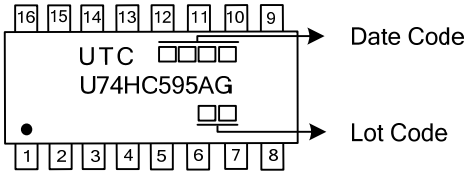
(1) T: Tube, R: Tape Reel
(2) D16: DIP-16, S16: SOP-16, P16: TSSOP-16
(3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING

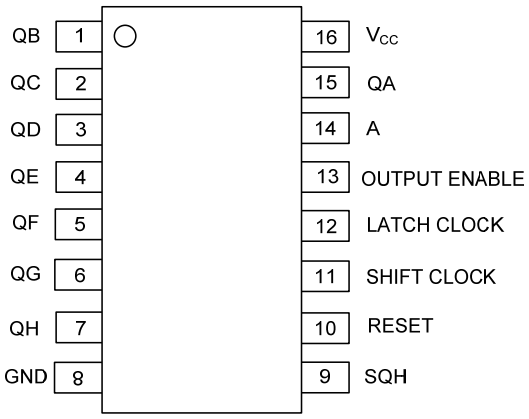
DIP-16



SOP-16 / TSSOP-16



■ PIN CONFIGURATION

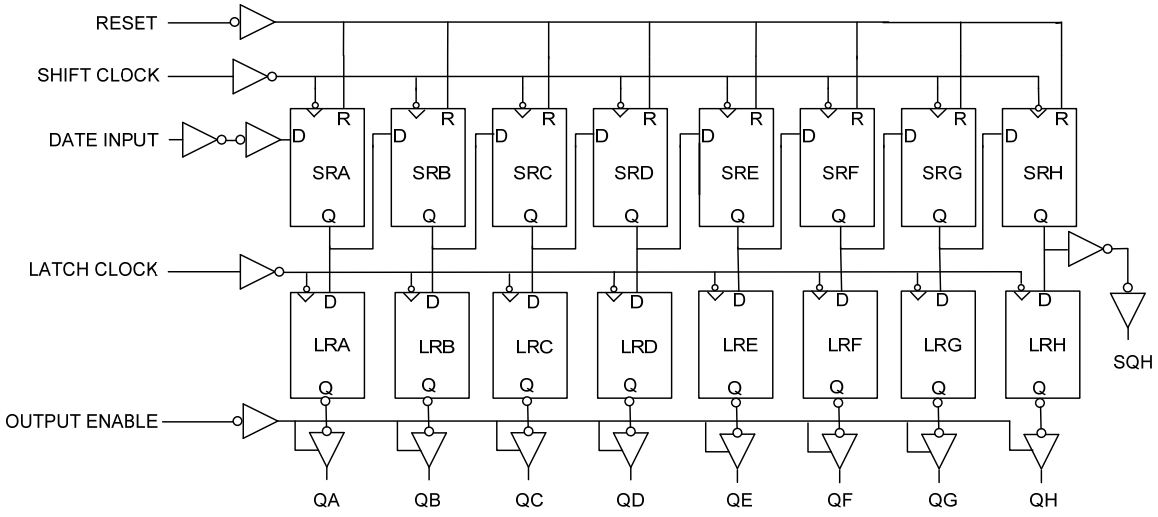


■ FUNCTION TABLE

Operation	INPUT					OUTPUT			
	Reset	Serial input A	Shift clock	Latch clock	Output enable	SR	LR	SQH	QA to QH
Reset shift register	L	X	X	L,H, ↓	L	L	NC	L	NC
Shift data into shift register	H	D	↑	L,H, ↓	L	D→ SR_A SR_N→SR_N+1	NC	SR_G→SR_H	NC
Shift register remains unchanged	H	X	L,H, ↓	L,H, ↓	L	NC	NC	NC	NC
Transfer shift register contents to latch register	H	X	L,H, ↓	↑	L	NC	SR_N→LR_N	NC	SR_N
Latch register remains unchanged	X	X	X	L,H, ↓	L	*	NC	*	NC
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR: shift register contents LR: latch register contents NC: unchanged
D: data(L,H) logic level ↑: low-to-high ↓: high-to-low
*: depends on Reset and Shift Clock inputs **: depends on Latch Clock inputs

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 2)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5~7.0	V
Input Voltage		V_{IN}	-0.5~Vcc+0.5	V
Output Voltage(active mode)		V_{OUT}	-0.5~V_{CC}+0.5	V
Input Clamp Current (V_{IN} <0)		I_{IK}	±20	mA
Output Clamp Current (V_{OUT} <0)		I_{OK}	±20	mA
Output Current		I_{OUT}	±35	mA
V_{CC} or GND Current		I_{CC}	±75	mA
Power Dissipation	DIP-16	P_D	750	mW
	SOP-16		500	
	TSSOP-16		450	
Storage Temperature		T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2		6	V
Input Voltage		V_{IN}	0		V_{CC}	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Operating Temperature		T_{OPR}	-40		125	°C
Input Transition Rise or Fall Rate	V_{CC} =2V	t_R / t_F			1000	ns
	V_{CC} =4.5V				500	ns
	V_{CC} =6V				400	ns

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-level input voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=3V	2.1			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
LOW-lever output voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=3V			0.9	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
High-Level Output Voltage, QA-QH	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4			V
		V_{CC}=6V, I_{OH}=-20μA	5.9			V
		V_{CC}=3V, I_{OH}=-2.4mA	2.48			V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98			V
		V_{CC}=6V, I_{OH}=-7.8mA	5.48			V
Low-Level Output Voltage, QA-QH	V_{OL}	V_{CC}=2V, I_{OL}=20μA			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA			0.1	V
		V_{CC}=6V, I_{OL}=20μA			0.1	V
		V_{CC}=3V, I_{OL}=2.4mA			0.26	V
		V_{CC}=4.5V, I_{OL}=6mA			0.26	V
		V_{CC}=6V, I_{OL}=7.8mA			0.26	V
High-Level Output Voltage, SQH	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4			V
		V_{CC}=6V, I_{OH}=-20μA	5.9			V
		V_{CC}=3V, I_{OH}=-2.4mA	2.48			V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98			V
		V_{CC}=6V, I_{OH}=-5.2mA	5.48			V
Low-Level Output Voltage, SQH	V_{OL}	V_{CC}=2V, I_{OL}=20μA			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA			0.1	V
		V_{CC}=6V, I_{OL}=20μA			0.1	V
		V_{CC}=3V, I_{OL}=2.4mA			0.26	V
		V_{CC}=4.5V, I_{OL}=4mA			0.26	V
		V_{CC}=6V, I_{OL}=5.2mA			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}=V_{CC} or GND			±0.1	μA
Output OFF -state current	I_{OZ}	V_{CC}=6V, V_{OUT}=V_{CC} or GND			±0.5	μA
Quiescent Supply Current	I_Q	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	μA
Input Capacitance	C_{IN}	V_{CC}=6V, V_{IN}=V_{CC} or GND			10	pF

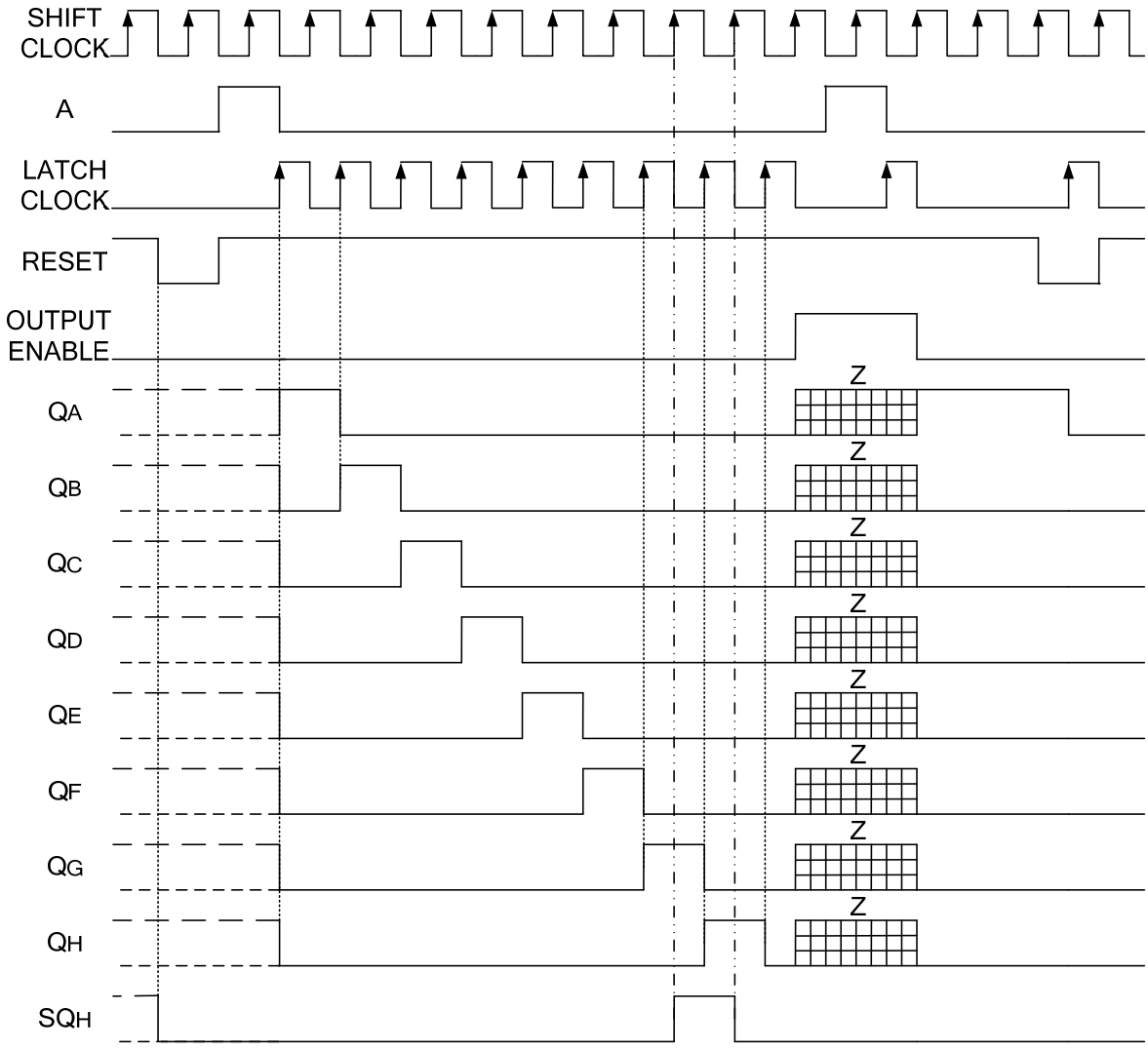
■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{max}	V_{CC}=2V			6	MHz
		V_{CC}=3V			15	MHz
		V_{CC}=4.5V			30	MHz
		V_{CC}=6V			35	MHz
Propagation delay from input (Latch Clock) to output(Qn)	t_{PHL}/t_{PLH}	V_{CC}=2V			140	ns
		V_{CC}=3V			100	ns
		V_{CC}=4.5V			28	ns
		V_{CC}=6V			24	ns
Propagation delay from input (Output Enable) to output(Qn)	t_{PZL}/t_{PZH}	V_{CC}=2V			135	ns
		V_{CC}=3V			90	ns
		V_{CC}=4.5V			27	ns
		V_{CC}=6V			23	ns
Propagation delay from input (Output Enable) to output(Qn)	t_{PLZ}/t_{PHZ}	V_{CC}=2V			150	ns
		V_{CC}=3V			100	ns
		V_{CC}=4.5V			30	ns
		V_{CC}=6V			26	ns
Output transition time, SQH	t_{TLH}/t_{THL}	V_{CC}=2V			75	ns
		V_{CC}=3V			27	ns
		V_{CC}=4.5V			15	ns
		V_{CC}=6V			13	ns
Propagation delay from input (Reset) to output(SQH)	t_{PHL}	V_{CC}=2V			145	ns
		V_{CC}=3V			100	ns
		V_{CC}=4.5V			29	ns
		V_{CC}=6V			25	ns
Propagation delay from input (Shift Clock) to output(SQH)	t_{PLH}/t_{PHL}	V_{CC}=2V			140	ns
		V_{CC}=3V			100	ns
		V_{CC}=4.5V			28	ns
		V_{CC}=6V			24	ns
Output transition time, Qn	t_{TLH}/t_{THL}	V_{CC}=2V			60	ns
		V_{CC}=3V			23	ns
		V_{CC}=4.5V			12	ns
		V_{CC}=6V			10	ns

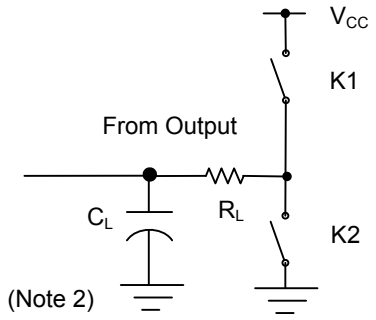
■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	No load		300		pF

■ TIMING DIAGRAM



■ TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Close	Open
t_{PLZ}/t_{PZL}	Open	Close

Note 2: CL includes probe and jig capacitance. C_L=50pF, R_L=1KΩ