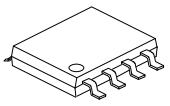
# FAIL-SAFE, 500KBPS, RS-485 / RS-422 TRANSCEIVERS WITH ±15KV ESD-PROTECTED



SOP-8

## ■ DESCRIPTION

The UTC **UTRS3085** high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. The device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be logic high if all transmitters on a terminated bus are disabled (high impedance). The UTC **UTRS3085** offer higher driver output slew-rate limits, allowing transmission up to 500kbps.

The transceiver typically draws 375μA of supply current when unloaded or when fully loaded with the drivers disabled.

A device has a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

## ■ FEATURES

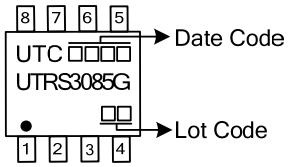
* True fail-safe receiver while maintaining EIA/TIA-485 compatibility.
* Enhanced slew-rate limiting facilitates Error-Free data transmission.
* 5.0V single power supply.
* 1μA low-current shutdown mode.
* Allow up to 256 transceivers on the Bus.
* HBM ±15kV ESD-protected.
* Driver short circuit current limit.
* Thermal shutdown for overload protection.

## ■ ORDERING INFORMATION

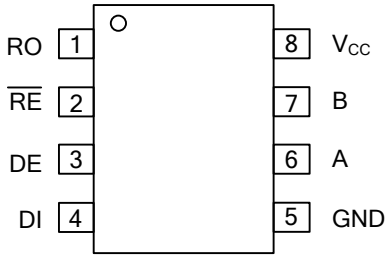
| Ordering Number | Package | Packing |
|---|---|---|
| UTRS3085G-S08-R | SOP-8 | Tape Reel |

| | |
|---|---|
| UTRS3085G-S08-R<br>(1)Packing Type<br>(2)Package Type<br>(3)Green Package | (1) R: Tape Reel<br>(2) S08: SOP-8<br>(3) G: Halogen Free and Lead Free |

## ■ MARKING



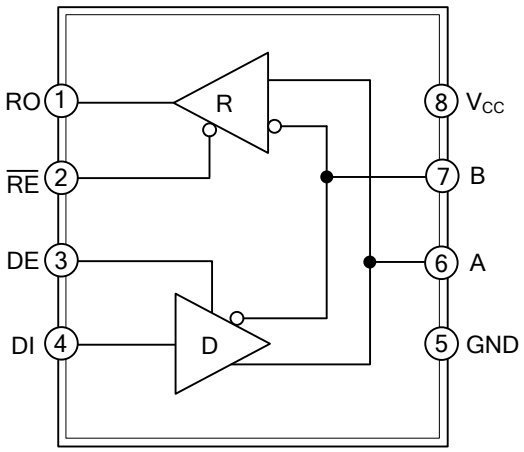
## ■ PIN CONFIGURATION




## ■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | RO | Receiver output. |
| 2 | $\overline{RE}$ | Receiver output enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. |
| 3 | DE | Driver output enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. |
| 4 | DI | Driver input. With DE high, a low on DI forces non-inverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low. |
| 5 | GND | Ground |
| 6 | A | Non-inverting receiver input and non-inverting driver output |
| 7 | B | Inverting receiver input and inverting driver output |
| 8 | $V_{CC}$ | Positive supply, $4.75V \le V_{CC} \le 5.25V$ |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | +7.0 | V |
| Control Input Voltage ($\overline{RE}$, DE) | | | -0.3~($V_{CC}$+0.3) | V |
| Special Input Voltage (H/$\overline{F}$, SRL, TXP, RXP). | | | -0.3~($V_{CC}$+0.3) | V |
| Driver Input Voltage | | DI | -0.3~($V_{CC}$+0.3) | V |
| Driver Output Voltage (A, B, Y, Z) | | | ±13 | V |
| Receiver Input Voltage (A, B) | | | ±13 | V |
| Receiver Input Voltage, Full Duplex (A, B) | | | ±25 | V |
| Receiver Output Voltage (RO) | | | -0.3~($V_{CC}$+0.3) | V |
| Continuous Power Dissipation | Derate 5.88mW/°C above +70°C | | 471 | mW |
| Operating Temperature Ranges | | $T_{OPR}$ | -40~+85 | °C |
| Storage Temperature Range | | $T_{STG}$ | -65~+150 | °C |
| Lead Temperature (Soldering, 10sec) | | $T_L$ | +300 | °C |

Note: Absolute maximum ratings are only stress ratings and it is not implied for functional device operation. Absolute maximum ratings are the values beyond which the device will be damaged permanently.

## ■ DC ELECTRICAL CHARACTERISTICS

($V_{CC}$=+5.0V ±5%, $T_A$=$T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$=+5.0V and $T_A$=+25°C) (Note 1)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | | |
| Differential Driver Output (No Load) | $V_{OD1}$ | Fig.1 | | | | 5.0 | V |
| Differential Driver Output | $V_{OD2}$ | Fig.1, R=50Ω (RS-422) | | 1.8 | | | V |
| | | Fig.1, R=27Ω (RS-485) | | 1.2 | | | V |
| Change in Magnitude of Differential Output Voltage (Note 2) | $\Delta V_{OD}$ | Fig.1, R=50Ω or R=27Ω | | | | 0.2 | V |
| Driver Common-Mode Output Voltage | $V_{OC}$ | Fig.1, R=50Ω or R=27Ω | | | | 3 | V |
| Change In Magnitude of Common-Mode Voltage (Note 2) | $\Delta V_{OC}$ | Fig.1, R=50Ω or R=27Ω | | | | 0.2 | V |
| Input High Voltage | $V_{IH1}$ | DE, DI, $\overline{RE}$, H/$\overline{F}$, TXP, RXP | | 2.0 | | | V |
| Input Low Voltage | $V_{IL1}$ | DE, DI, $\overline{RE}$, H/$\overline{F}$, TXP, RXP | | | | 0.8 | V |
| DI Input Hysteresis | $V_{HYS}$ | SRL=$V_{CC}$ or Unconnected | | | 100 | | mV |
| SRL Input Current | $I_{IN1}$ | DE, DI, $\overline{RE}$ | | | | ±2 | μA |
| | $I_{IN2}$ | H/$\overline{F}$, TXP, RXP, Internal Pull-down | | 10 | | 40 | μA |
| Input High Voltage | $V_{IH2}$ | SRL | | $V_{CC}$-0.8 | | | V |
| Input Middle Voltage | $V_{IM2}$ | SRL (Note 3) | | 0.4$V_{CC}$ | | 0.6$V_{CC}$ | V |
| Input Low Voltage | $V_{IL2}$ | SRL | | | | 0.8 | V |
| SRL Input Current | $I_{IN3}$ | SRL=$V_{CC}$ | | | | 75 | μA |
| | | SRL=GND (Note 3) | | -75 | | | μA |
| Input Current (A and B) Full Duplex | $I_{IN4}$ | DE=GND, $V_{CC}$=GND or 5.25V | $V_{IN}$=12V | | | 125 | μA |
| | | | $V_{IN}$=-7V | | | -75 | μA |
| Output Leakage (Y and Z) Full Duplex | $I_O$ | DE=GND, VCC=GND or 5.25V | $V_{IN}$=12V | | | 125 | μA |
| | | | $V_{IN}$=-7V | -100 | | | μA |
| Driver Short-Circuit Output Current (Note 4) | $V_{OD1}$ | -7V≤$V_{OUT}$≤$V_{CC}$ | | -250 | | | mA |
| | | 0V≤$V_{OUT}$≤12V | | | | 250 | mA |
| | | 0V≤$V_{OUT}$≤$V_{CC}$ | | ±25 | | | mA |

## ■ DC ELECTRICAL CHARACTERISTICS (Cont.)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **RECEIVER** | | | | | | | |
| Receiver Differential Threshold Voltage | $V_{TH}$ | -7V≤$V_{CM}$≤+12V | | | -300 | | mV |
| Receiver Input Hysteresis | $\Delta V_{TH}$ | | | | 25 | | mV |
| Receiver Output High Voltage | $V_{OH}$ | $I_O$=-4mA, $V_{ID}$=-50mV | | $V_{CC}$-1.5 | | | V |
| Receiver Output Low Voltage | $V_{OL}$ | $I_O$=4mA, $V_{ID}$=-200mV | | | | 0.4 | V |
| Three-State Output Current at Receiver | $I_{OZR}$ | 0.4V≤$V_O$≤2.4V | | | | ±1 | μA |
| Receiver Input Resistance | $R_{IN}$ | -7V≤$V_{CM}$≤+12V | | 96 | | | kΩ |
| Receiver Output Short-Circuit Current | $I_{OSR}$ | 0V≤$V_{RO}$≤$V_{CC}$ | | ±7 | | ±95 | mA |
| **SUPPLY CURRENT** | | | | | | | |
| Supply Current | $I_{CC}$ | No Load, $\overline{RE}$ =DI=GND or $V_{CC}$, SRL=$V_{CC}$ | DE=$V_{CC}$ | | 430 | 900 | μA |
| | | | DE=GND | | 375 | 600 | μA |
| | | No Load, $\overline{RE}$ =DI=GND or $V_{CC}$, SRL=GND | DE=$V_{CC}$ | | 475 | 1000 | μA |
| | | | DE=GND | | 420 | 800 | μA |
| Supply Current in Shutdown Mode | $I_{SHDN}$ | DE=GND, $V_{\overline{RE}}$ =$V_{CC}$ | | | 1 | 10 | μA |

Notes: 1. All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.
2. $\Delta V_{OD}$ and $\Delta V_{OC}$ are the changes in $V_{OD}$ and $V_{OC}$, respectively, when the DI input changes state.
3. The SRL pin is internally biased to $V_{CC}$/ 2 by a 100kΩ/100kΩ resistor divider. It is guaranteed to be $V_{CC}$/ 2 if left unconnected.
4. Maximum current level applies to peak current just prior to foldback-current limiting; minimum current level applies during current limiting.

## ■ SWITCHING CHARACTERISTICS

($V_{CC}$=+5.0V ±5%, $T_A$=$T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{CC}$=+5.0V and $T_A$=+25°C)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Driver Input to Output | $t_{DPLH}$ | Fig.3 and 5, $R_{DIFF}$=54Ω, $C_{L1}$=$C_{L2}$=100pF | | 100 | | ns |
| | $t_{DPHL}$ | | | 100 | | ns |
| Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$ | $t_{DSKEW}$ | Fig.3 and 5, $R_{DIFF}$=54Ω, $C_{L1}$=$C_{L2}$=100pF | | -3 | ±100 | ns |
| Driver Rise or Fall Time | $t_{DR}$, $t_{DF}$ | Fig.3 and 5, $R_{DIFF}$=54Ω, $C_{L1}$=$C_{L2}$=100pF | | 200 | | ns |
| Maximum Data Rate | $f_{MAX}$ | | 500 | | | kbps |
| Driver Enable to Output High | $t_{DZH}$ | Fig.4 and 6, $C_L$=100pF, S2 Closed | | | 2500 | ns |
| Driver Enable to Output Low | $t_{DZL}$ | Fig.4 and 6, $C_L$=100pF, S1 Closed | | | 2500 | ns |
| Driver Disable Time from Low | $t_{DLZ}$ | Fig.4 and 6, $C_L$=15pF, S1 Closed | | | 100 | ns |
| Driver Disable Time from High | $t_{DHZ}$ | Fig.4 and 6, $C_L$=15pF, S2 Closed | | | 100 | ns |
| Receiver Input to Output | $t_{RPLH}$, $t_{RPHL}$ | Fig.7 and 9, $\lvert V_{ID} \rvert$≥2.0V; Rise and Fall Time of $V_{ID}$≤15ns | | 200 | | ns |
| $\lvert t_{RPLH} - t_{RPHL} \rvert$ Differential Receiver Skew | $t_{RSKD}$ | Fig.7 and 9, $\lvert V_{ID} \rvert$≥2.0V; Rise and Fall Time of $V_{ID}$≤15ns | | 50 | | ns |
| Receiver Enable to Output Low | $t_{RZL}$ | Fig.2 and 8, $C_L$=100pF, S1 Closed | | 100 | | ns |
| Receiver Enable to Output High | $t_{RZH}$ | Fig.2 and 8, $C_L$=100pF, S2 Closed | | 60 | | ns |
| Receiver Disable Time from Low | $t_{RLZ}$ | Fig.2 and 8, $C_L$=100pF, S1 Closed | | 300 | | ns |
| Receiver Disable Time from High | $t_{RHZ}$ | Fig.2 and 8, $C_L$=100pF, S2 Closed | | 200 | | ns |
| Time to Shutdown | $t_{SHDN}$ | Note 1 | | 200 | | ns |
| Driver Enable from Shutdown to Output High | $t_{DZH(SHDN)}$ | Fig.4 and 6, $C_L$=15pF, S2 Closed | | | 4500 | ns |
| Driver Enable from Shutdown to Output Low | $t_{DZL(SHDN)}$ | Fig.4 and 6, $C_L$=15pF, S1 Closed | | | 4500 | ns |
| Receiver Enable from Shutdown to Output High | $t_{RZH(SHDN)}$ | Fig.2 and 8, $C_L$=100pF, S2 Closed | | | 3500 | ns |
| Receiver Enable from Shutdown to Output Low | $t_{RZL(SHDN)}$ | Fig.2 and 8, $C_L$=100pF, S1 Closed | | | 3500 | ns |

Note: The device is put into shutdown by bringing $\overline{RE}$ high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

## ■ FUNCTION TABLE

TRANSMITTING

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{RE}$ | DE | DI | B/Z | A/Y |
| X | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 0 |
| 0 | 0 | X | High-Z | High-Z |
| 1 | 0 | X | Shutdown | |

RECEIVING

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{RE}$ | DE | A-B | RO |
| 0 | X | ≥-0.05V | 1 |
| 0 | X | ≤-0.2V | 0 |
| 0 | X | Open/Shorted | 1 |
| 1 | 1 | X | High-Z |
| 1 | 0 | X | Shutdown |

X = Don’t care

Shutdown mode, driver and receiver outputs high impedance

## ■ TEST CIRCUIT

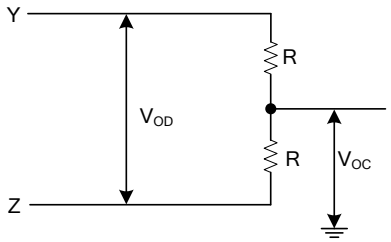



Fig. 1 Driver DC Test Circuit

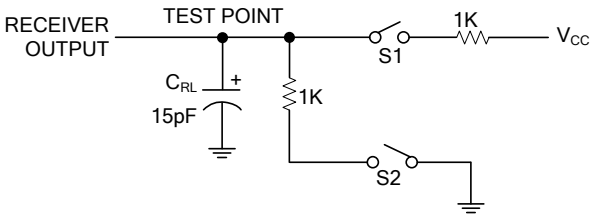



Fig. 2 Receiver Enable/Disable Timing Test Load

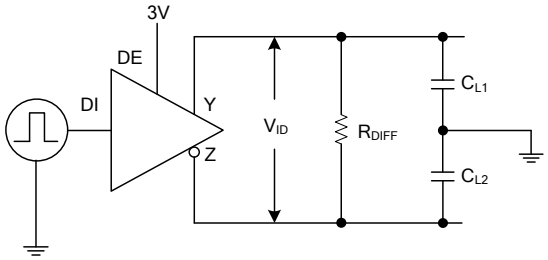



Fig. 3 Driver Timing Test Circuit

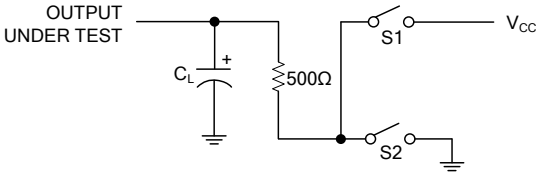



Fig. 4 Driver Enable/Disable Timing Test Load

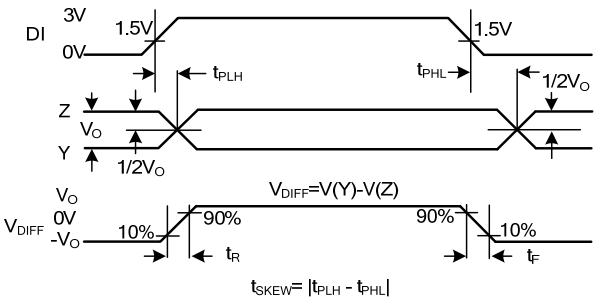



Fig. 5 Driver Propagation Delays

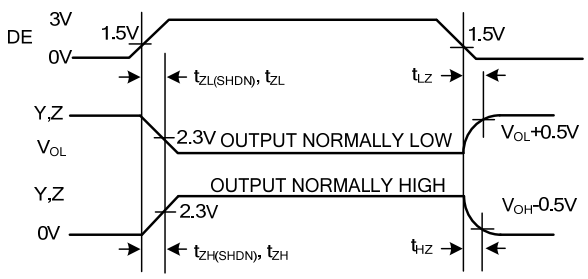



Fig. 6 Driver Enable and Disable Times

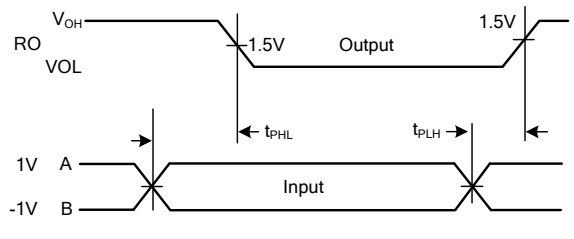



Fig. 7 Receiver Propagation Delays

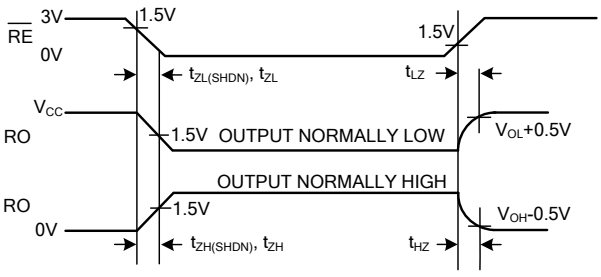



Fig. 8 Receiver Enable and Disable Times

## ■ TEST CIRCUIT (Cont.)

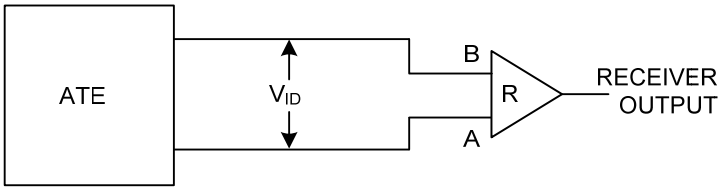
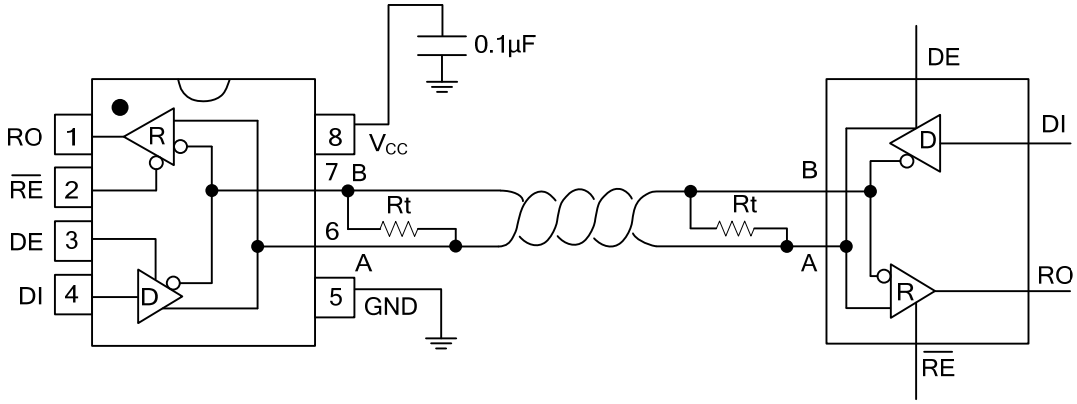



Fig. 9 Receiver Propagation Delay Test Circuit

## ■ TYPICAL APPLICATION CIRCUIT




Note: Pin labels Y and Z on timing, test, and waveform diagrams refer to pins A and B when DE is high.