

**UTRS485**

Preliminary

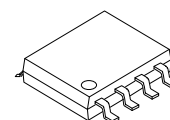
CMOS IC

**FAIL-SAFE, 2.5MBPS, RS-485 /
RS-422 TRANSCEIVERS WITH
±15KV ESD-PROTECTED****■ DESCRIPTION**

The UTC **UTRS485** is a half-duplex transceiver designed for RS-485 data bus network, which contains one transmitter and one receiver. The UTC **UTRS485** features a fail-safe receiver, which guarantees the receiver to output high when the receiver inputs are open, short or idle.

The UTC **UTRS485** also features a hot-swap glitch free protection circuits which guarantee outputs of both the transmitter and the receiver in a high impedance state during the power up period. So that the large short current from power to ground will be disable by glitch free function, which will save the power and enhance the efficiency of the power up.

The UTC **UTRS485** is optimized for signal rates up to 2.5Mbps with differential voltage of 2.3V. The UTC **UTRS485** also has the thermal shutdown function when the temperature is over 150°C and the protection of the current limitation in the transmitter to protect the itself from the damage by the system-fault conditions during normal operation.



SOP-8

■ FEATURES

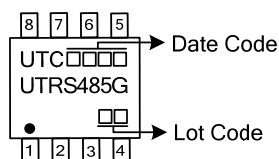
- * Meet the requirements of the EIA/TIA-485 standards.
- * 5.0V single power supply.
- * True fail-safe receiver while maintaining EIA/TIA-485 compatibility.
- * Hot-Swap glitch free protection on control inputs.
- * Up to 256 transceivers on the bus.
- * Driver short circuit current limit.
- * Thermal shutdown for overload protection.

■ ORDERING INFORMATION

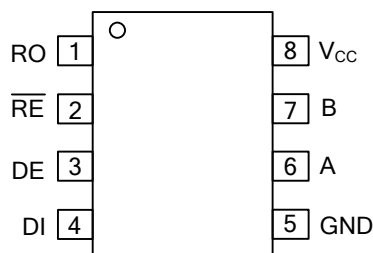
Ordering Number	Package	Packing
UTRS485G-S08-R	SOP-8	Tape Reel

UTRS485G-S08-R	
(1) Packing Type	(1) R: Tape Reel
(2) Package Type	(2) S08: SOP-8
(3) Green Package	(3) G: Halogen Free and Lead Free

MARKING



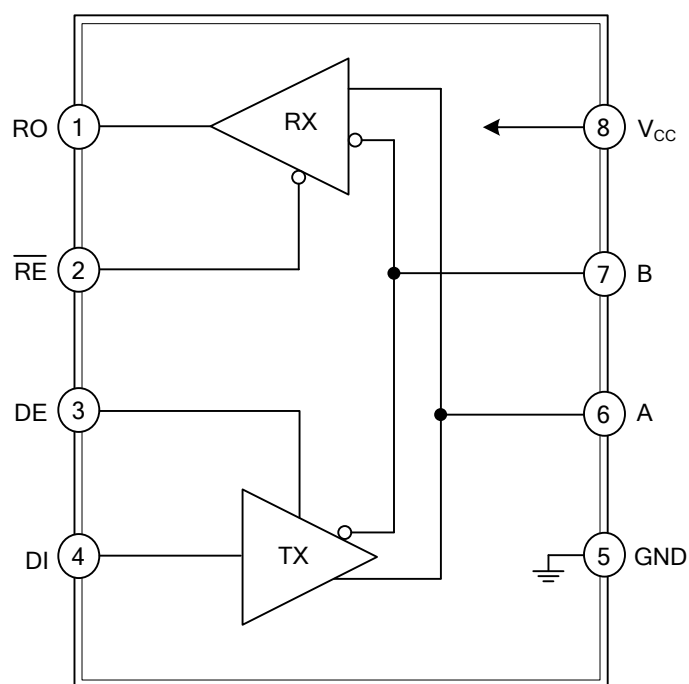
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	RO	Receiver output: if $A > B$ by 200mV, RO will be high; if $A < B$ by 200mV, RO will be low.
2	$\overline{RE}$	Receiver output enable. RO is enable when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	GND	Ground
6	A	Non-inverting receiver input and non-inverting driver output
7	B	Inverting receiver input and inverting driver output
8	V_{CC}	Positive supply; $4.75V \leq V_{CC} \leq 5.25V$

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	12	V
Control Input Voltage ($\overline{RE}$, DE)		$-0.5 \sim (V_{CC}+0.5)$	V
Driver Input Voltage (DI)	DI	$-0.5 \sim (V_{CC}+0.5)$	V
Driver Output Voltage (A, B)		$-8 \sim +12.5$	V
Receiver Input Voltage (A, B)		$-8 \sim +12.5$	V
Receiver Output Voltage (RO)		$-0.5 \sim (V_{CC}+0.5)$	V
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	Derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$	471	mW
Lead Temperature (Soldering, 10sec)	T_L	+300	$^\circ\text{C}$
Operating Temperature Ranges	T_{OPR}	$-40 \sim +85$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-65 \sim +160$	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0\text{V} \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. (Note 1, 2))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Driver Output (No Load)	V_{OD1}				5.0	V
Differential Driver Output (with Load)	V_{OD2}	$R = 50\Omega$ (RS-422) Fig.1, $R = 27\Omega$ (RS-485)	2.0 1.5		5	V
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	Fig.1, $R = 27\Omega$ or 50Ω			0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Fig.1, $R = 27\Omega$ or 50Ω			3.0	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	Fig.1, $R = 27\Omega$ or 50Ω			0.2	V
Input High Voltage	V_{IH1}	DE, DI, $\overline{RE}$	2.0			V
Input Low Voltage	V_{IL1}	DE, DI, $\overline{RE}$			0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$			± 2.0	μA
Input Current (A, B)	I_{IN2}	DE=0V; $V_{CC}=0\text{V}$ or 5.25V	$V_{IN}=12\text{V}$ $V_{IN}=-7\text{V}$		1.0 -0.8	mA
Receiver Differential Threshold Voltage	V_{TH}	$-7\text{V} \leq V_{CM} \leq +12\text{V}$	-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	$V_{CM}=0\text{V}$		70		mV
Receiver Output High Voltage	V_{OH}	$I_O = -4\text{mA}$, $V_{ID} = 200\text{mV}$	3.5			V
Receiver Output Low Voltage	V_{OL}	$I_O = 4\text{mA}$, $V_{ID} = -200\text{mV}$			0.5	V
Three-State (High Impedance) Output Current at Receiver	I_{OZR}	$0.4\text{V} \leq V_O \leq 2.4\text{V}$			± 1.0	μA
Receiver Input Resistance	R_{IN}	$-7\text{V} \leq V_{CM} \leq +12\text{V}$	12			k Ω
No-Load Supply Current (Note 3)	I_{CC}	$\overline{RE} = 0\text{V}$ or V_{CC}	DE= V_{CC} DE=0V	500 300	900 500	μA
Driver Short-Circuit Current, $V_O = \text{High}$	I_{OSD1}	$-7\text{V} \leq V_O \leq 12\text{V}$ (Note 4)	35		250	mA
Driver Short-Circuit Current, $V_O = \text{Low}$	I_{OSD2}	$-7\text{V} \leq V_O \leq 12\text{V}$ (Note 4)	35		250	mA
Receiver Short-Circuit Current	I_{OSR}	$0\text{V} \leq V_O \leq V_{CC}$	7		95	mA

■ SWITCHING CHARACTERISTICS

($V_{CC}=+5.0V \pm 5\%$, $T_A=T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Note 1, 2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Input to Output	t_{PLH}	Fig.3 and 5, $R_{DIFF}=54\Omega$, $C_{L1}=C_{L2}=100pF$	10	50	100	ns
	t_{PHL}		10	50	100	ns
Driver Output Skew to Output	t_{SKEW}	Fig.3 and 5, $R_{DIFF}=54\Omega$, $C_{L1}=C_{L2}=100pF$		10		ns
Driver Rise or Fall Time	t_{DR} , t_{DF}	Fig.3 and 5, $R_{DIFF}=54\Omega$, $C_{L1}=C_{L2}=100pF$	3	15	40	ns
Driver Enable to Output High	t_{ZH}	Fig.4 and 6, $C_L=100pF$, S2 Closed		80	150	ns
Driver Enable to Output Low	t_{ZL}	Fig.4 and 6, $C_L=100pF$, S1 Closed		80	150	ns
Driver Disable Time from Low	t_{LZ}	Fig.4 and 6, $C_L=15pF$, S1 Closed		80	150	ns
Driver Disable Time from High	t_{HZ}	Fig.4 and 6, $C_L=15pF$, S2 Closed		80	150	ns
Receiver Input to Output	t_{PLH} , t_{PHL}	Fig.3 and 7, $R_{DIFF}=54\Omega$, $C_{L1}=C_{L2}=100pF$	20	500	1000	ns
$ t_{PLH} - t_{PHL} $ Differential Receiver Skew	t_{SKD}	Fig.3 and 7, $R_{DIFF}=54\Omega$, $C_{L1}=C_{L2}=100pF$		100		ns
Receiver Enable to Output Low	t_{ZL}	Fig.2 and 8, $C_{RL}=15pF$, S1 Closed		30	60	ns
Receiver Enable to Output High	t_{ZH}	Fig.2 and 8, $C_{RL}=15pF$, S2 Closed		30	60	ns
Receiver Disable Time from Low	t_{LZ}	Fig.2 and 8, $C_{RL}=15pF$, S1 Closed		30	60	ns
Receiver Disable Time from High	t_{HZ}	Fig.2 and 8, $C_{RL}=15pF$, S2 Closed		30	60	ns

Notes: 1. All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground unless otherwise specified.

2. All typical specifications are given for $V_{CC}=5V$ and $T_A=+25^\circ C$

3. Supply current specification is valid for loaded transmitters when $DE=0V$

4. Applies to peak current

■ FUNCTION TABLE

Table 1 TRANSMITTING

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z	High-Z

Table 2 RECEIVING

INPUTS			OUTPUTS
$\overline{RE}$	DE	A-B	RO
0	0	$\geq +0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs open	1
1	0	X	High-Z

X = Don't care

High-Z = High impedance

■ TEST CIRCUIT

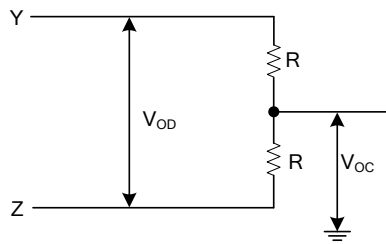


Fig. 1 Driver DC Test Load

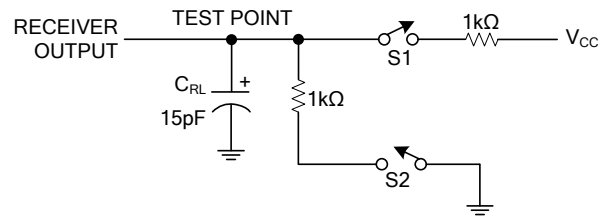


Fig. 2 Receiver Timing Test Load

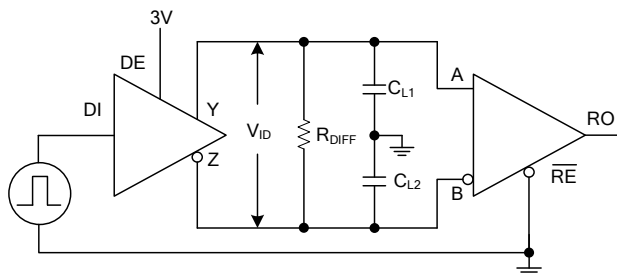


Fig. 3 Driver/Receiver Timing Test Circuit

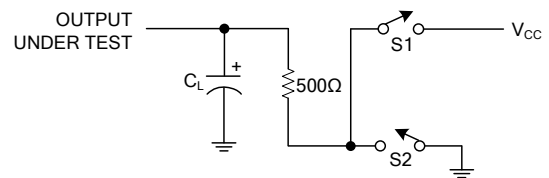


Fig. 4 Driver Timing Test Load

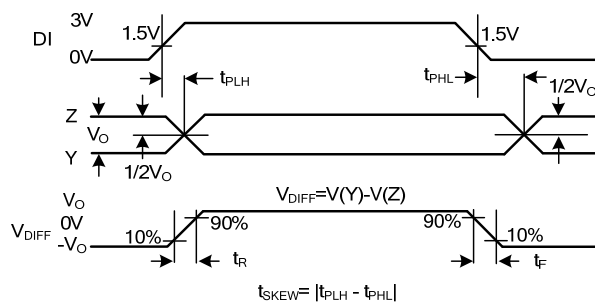


Fig. 5 Driver Propagation Delays

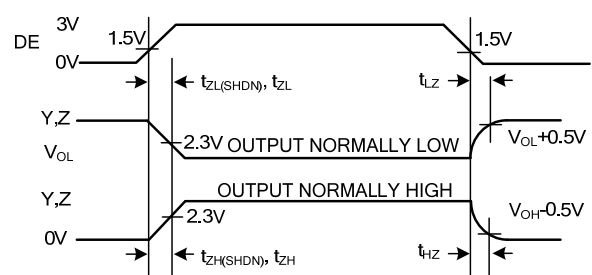


Fig. 6 Driver Enable and Disable Times

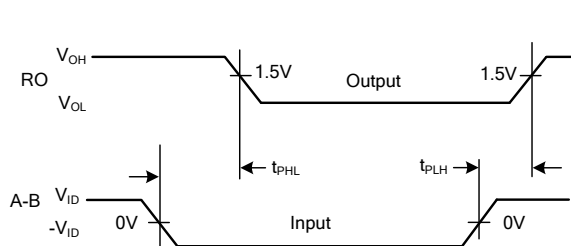


Fig. 7 Receiver Propagation Delays

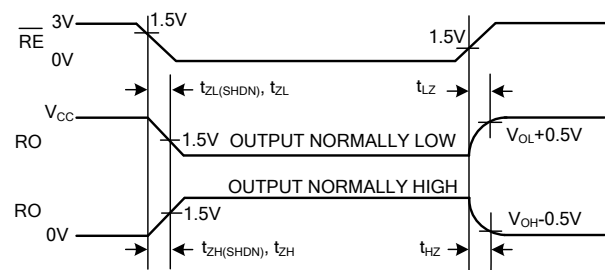
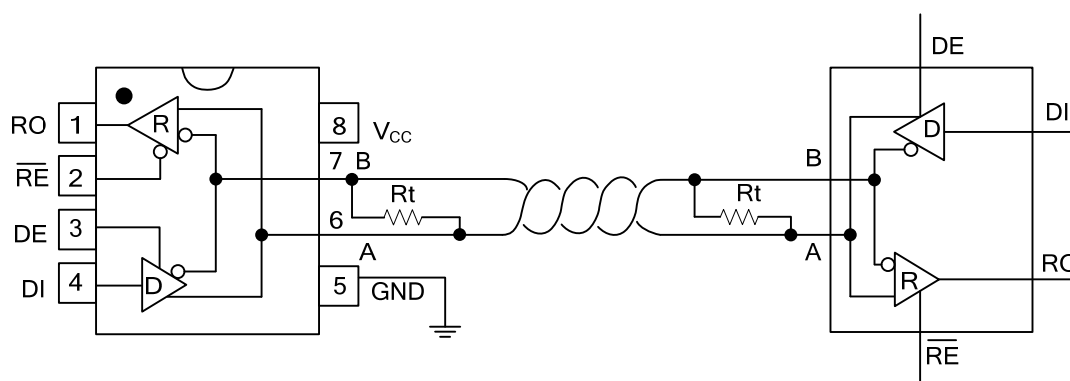


Fig. 8 Receiver Enable and Disable Times

■ TYPICAL APPLICATION CIRCUIT



Note: Pin labels Y and Z on timing, test, and waveform diagrams refer to pins A and B when DE is high.

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