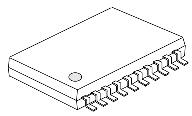
EXPRESSCARD^{TM} POWER INTERFACE SWITCH



TSSOP-20

DESCRIPTION

The UTC **US12231** ExpressCard^{TM} power interface switches are designed to meet the ExpressCard^{TM} specification. The UTC **US12231** distribute 3.3V, AUX, and 1.5V to the single-slot ExpressCard|34 or ExpressCard|54 sockets. Each voltage rail is protected with integrated current-limiting circuitry, other functions include thermal protection circuit turns off switches to prevent device from damage when heavy overloads or short circuits,

The UTC **US12231** can use in notebook computers, desktop computers, PDAs, and digital cameras.

FEATURES

* Meets the ExpressCard^{TM} standard (ExpressCard|34 or ExpressCard|54)
* Compliant with the ExpressCard^{TM} compliance checklists
* Fully satisfies the ExpressCard^{TM} implementation guidelines
* Supports systems with WAKE function
* TTL-Logic compatible inputs
* Short circuit and thermal protection
* -40°C ~ 85°C ambient operating temperature range

ORDERING INFORMATION

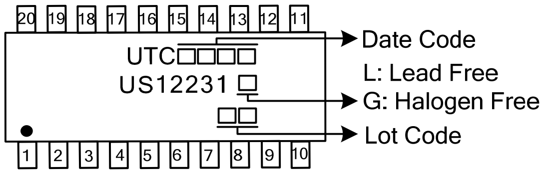
Ordering Number		Package	Packing
Lead Free	Halogen Free		
US12231L-P20-T	US12231G-P20-T	TSSOP-20	Tube
US12231L-P20-R	US12231G-P20-R	TSSOP-20	Tape Reel

US12231L-P20-T

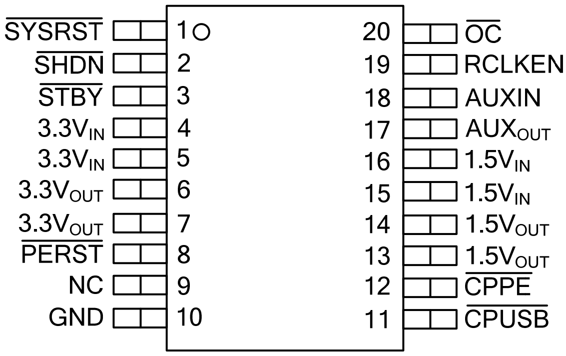
(1)Packing Type	(1) T: Tube, R: Tape Reel
(2)Package Type	(2) P20: TSSOP-20
(3)Lead Free	(3) L: Lead Free, G: Halogen Free

※ ExpressCard is a trademark of Personal Computer Memory Card International Association.

■ MARKING INFORMATION

PACKAGE	MARKING
TSSOP-20	

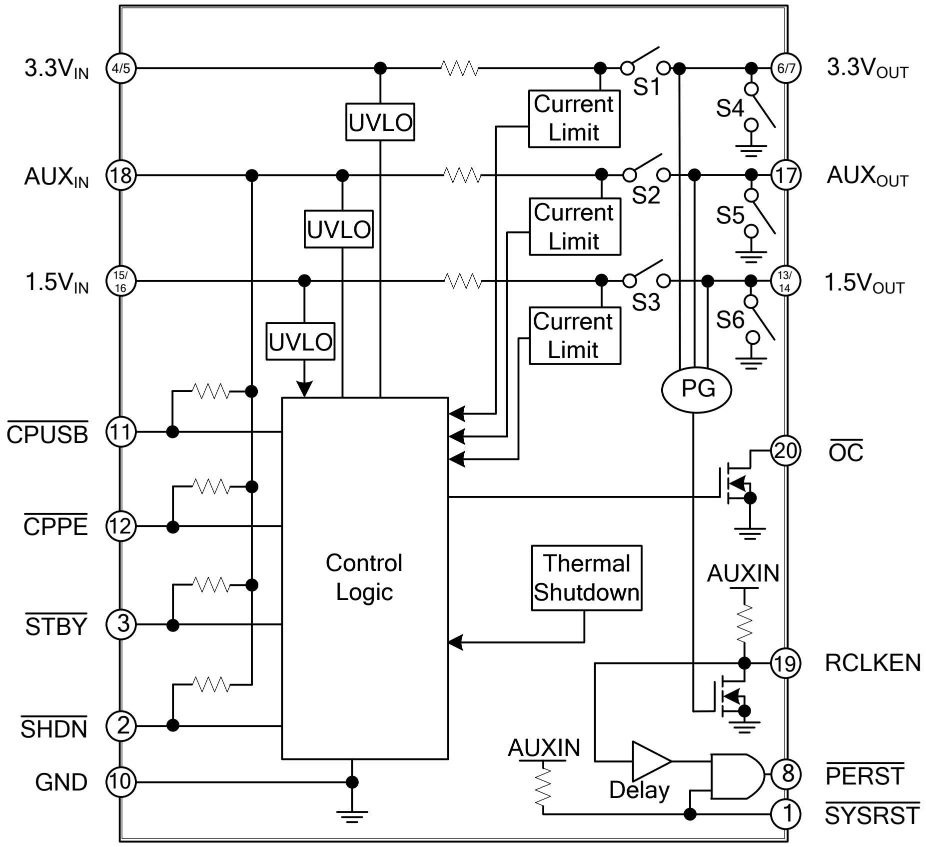
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	$\overline{SYSRST}$	I	System Reset input – active low, logic level signal. Internally pulled up to AUXIN.
2	$\overline{SHDN}$	I	Shutdown input – active low, logic level signal. Internally pulled up to AUXIN.
3	$\overline{STBY}$	I	Standby input – active low, logic level signal. Internally pulled up to AUXIN.
4, 5	$3.3V_{IN}$	I	3.3-V input for 3.3VOUT
6, 7	$3.3V_{OUT}$	O	Switched output that delivers 0 V, 3.3 V or high impedance to card
8	$\overline{PERST}$	O	A logic level power good to slot 0 (with delay)
9	NC		No connection
10	GND		Ground
11	$\overline{CPUSB}$	I	Card Present input for USB cards. Internally pulled up to AUXIN.
12	$\overline{CPPE}$	I	Card Present input for PCI Expresscards™. Internally pulled up to AUXIN
13, 14	$1.5V_{OUT}$	O	Switched output that delivers 0 V, 1.5 V or high impedance to card
15,16	$1.5V_{IN}$	I	1.5-V input for 1.5VOUT
17	AUX_{OUT}	O	Switched output that delivers 0 V, AUX or high impedance to card
18	AUX_{IN}	I	AUX input for AUXOUT and chip power
19	RCLKEN	I/O	Reference Clock Enable signal. As an output, a logic level power good to host for slot 0 (no delay – open drain). As an input, if kept inactive (low) by the host, prevents $\overline{PERST}$ from being de-asserted. Internally pulled up to AUXIN.
20	$\overline{OC}$	O	Overcurrent status output for slot 0 (open drain)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Input Voltage Range For Card Power	V_{IN}	$1.5V_{IN}$	-0.3~6	V
		$3.3V_{IN}$	-0.3~6	
		AUX_{IN}	-0.3~6	
Logic Input/Output Voltage			-0.3~6	V
Output Voltage Range	V_{OUT}	$1.5V_{IN}$	-0.3~6	V
		$3.3V_{IN}$	-0.3~6	
		AUX_{IN}	-0.3~6	
Continuous Total Power Dissipation			See dissipation rating table	
Output Current	I_{OUT}	$1.5V_{IN}$	Internally limited	
		$3.3V_{IN}$	Internally limited	
		AUX_{IN}	Internally limited	
$\overline{\text{OC}}$ Sink Current			10	mA
$\overline{\text{PERST}}$ Sink/Source Current			10	mA
Operating Virtual Junction Temperature Range	T_J		-40~+120	°C
Storage Temperature Range	T_{STG}		-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ DISSIPATION RATINGS (Thermal Resistance=°C/W)

PARAMETER	SYMBOL	RATINGS	UNIT
POWER RATING (T_A≤25°C)		704.2	mW

Note: These devices are mounted on a JEDEC low-k board (2-oz. traces on surface), (The table is assuming that the maximum junction temperature is 120°C).

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	$1.5V_{IN}$	$1.5V_{IN}$ is only required for its respective functions	1.35		1.65	V
		$3.3V_{IN}$	$3.3V_{IN}$ is only required for its respective functions	3		3.6	
		AUX_{IN}	AUX_{IN} is required for all circuit operations	3		3.6	
Continuous Output Current	I_{OUT}	$1.5V_{OUT}$		0		650	mA
		$3.3V_{OUT}$		0		1.3	A
		AUX_{OUT}		0		275	mA
Operating Virtual Junction Temperature	T_J			-40		120	°C

■ ELECTRICAL CHARACTERISTICS

T_J=25°C, $V_{I(3.3VIN)}$=$V_{I(AUXIN)}$=3.3V, $V_{I(1.5VIN)}$=1.5V, $V_{I(/SHDNx)}$, $V_{I(/STBYx)}$=3.3V, $V_{I(/CPPEx)}$=$V_{I(/CPUSBx)}$=0V, $V_{I(/SYSRST)}$=3.3V, $\overline{\text{OCx}}$ and RCLKENx and $\overline{\text{PERSTx}}$ are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER			SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Switch Resistance	$1.5V_{IN}$~$1.5V_{OUT}$		R_{DS}	T_J=25°C, I=650mA each		46		mΩ
				T_J=100°C, I=650mA each			70	
	$3.3V_{IN}$~$3.3V_{OUT}$			T_J=25°C, I=1300mA each		45		mΩ
				T_J=100°C, I=1300mA each			68	
	AUX_{IN}~AUX_{OUT}			T_J=25°C, I=275mA each		120		mΩ
				T_J=100°C, I=275mA each			200	
Discharge Resistance On 3.3V/1.5V/AUX Outputs			$R_{(DIS\_FET)}$	$V_{I(/SHDNx)}$=0V, $I_{(discharge)}$=1mA	100		500	Ω
Short -Circuit Output Current (Note 1)	Steady-State Value	$1.5V_{OUT}$	I_{OS}	T_J (-40~120°C), Output powered into a short	0.67	1	1.3	A
		$3.3V_{OUT}$			1.35	2	2.5	A
		AUX_{OUT}			275	450	600	mA
Thermal Shutdown	Trip Point, T_J		T_J	Rising temperature, not in overcurrent condition	155	165		°C
			T_{J_OC}	Overcurrent condition	120	130		
	Hysteresis		ΔT			10		°C
Current -Limit Response Time	From Short To The 1st Threshold Within 1.1Times Of Final Current Limit, T_J=25°C			$V_{O(3.3VOUT)}$ with 100-mΩ short		43	100	µs
				$V_{O(1.5VOUT)}$ with 100-mΩ short		100	140	
				$V_{O(AUXOUT)}$ with 100-mΩ short		38	100	
Operation Input Quiescent Current	Normal Operation	$1.5V_{IN}$	I_I	Outputs are unloaded, T_J (–40, 120°C) (does not include $\overline{\text{CPPEx}}$ and $\overline{\text{CPUSBx}}$ logic pullup currents)		2.5	10	µA
		$3.3V_{IN}$				10	15	
		AUX_{IN}				85	150	
Total Input Quiescent Current	Normal Operation	$1.5V_{IN}$	I_I	Outputs are unloaded, T_J (–40, 120°C) (include $\overline{\text{CPPEx}}$ and $\overline{\text{CPUSBx}}$ logic pullup currents)		2.5	10	µA
		$3.3V_{IN}$				10	15	
		AUX_{IN}				120	210	
	Shutdown Mode	$1.5V_{IN}$		$\overline{\text{CPUSB}}$ = $\overline{\text{CPPE}}$ =0V, $\overline{\text{SHDN}}$ =0V (discharge FETs are on) (include $\overline{\text{CPPEx}}$ and $\overline{\text{CPUSBx}}$ logic pullup currents and $\overline{\text{SHDN}}$ pullup current) T_J (–40, 120°C)		0.5	10	µA
		$3.3V_{IN}$				3.5	10	
		AUX_{IN}				144	270	
Forward Leakage Current		$1.5V_{IN}$	$I_{lkg(FWD)}$	$\overline{\text{SHDN}}$ =3.3V, $\overline{\text{CPUSB}}$ = $\overline{\text{CPPE}}$ = 3.3V (no card present, discharge FETs are on), current measured at input pins, T_J=120°C, includes RCLKEN pullup current		0.1	50	µA
		$3.3V_{IN}$				0.1	50	
		AUX_{IN}				20	50	
Reverse Leakage Current	T_J=25°C	$1.5V_{IN}$	$I_{lkg(RVS)}$	$V_{O(AUXOUT)}$=$V_{O(3.3VOUT)}$=3.3V, $V_{O(1.5VOUT)}$=1.5V, All voltage inputs are grounded (current measured from output pins going in)		0.1	10	µA
	T_J=120°C						50	
	T_J=25°C	$3.3V_{IN}$				0.1	10	µA
	T_J=120°C						50	
	T_J=25°C	AUX_{IN}				0.1	10	µA
	T_J=120°C						50	

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC SECTION (SYSRST , SHDNx , STBYx , PERSTx , RCLKENx, OCx , CPUSBx , CPPEx)							
Logic Input Supply Current	Input	$I_{(\overline{SYSRST})}$	SYSRST =3.6V, sinking		0	1	μA
	Input	$I_{(\overline{SYSRST})}$	SYSRST =0V, sourcing		0	1	μA
				10		30	
	Input	$I_{(\overline{SHDNx})}$	SHDNx =3.6V, sinking		0	1	μA
			SHDNx =0V, sourcing	10		30	
	Input	$I_{(\overline{STBYx})}$	STBYx =3.6V, sinking		0	1	μA
			STBYx =0V, sourcing	10		30	
	Input	$I_{(RCLKENx)}$	RCLKENx=0V, sourcing	10		30	μA
	Inputs	$I_{(\overline{CPUSBx})}$ Or $I_{(\overline{CPPEx})}$	CPUSB or CPPE =0V, sinking		0	1	μA
			CPUSB or CPPE =3.6V, sourcing	10		30	
Logic Input Voltage	High Level	V_{IH}		2			V
	Low Level	V_{IL}				0.8	
RCLEN Output Low Voltage	Output	$V_{OL(RCLEN)}$	$I_{O(RCLKEN)}$=60μA			0.4	V
PERST Assertion Threshold Of Output Voltage (PERST Asserted When Any Output Voltage Falls Below The Threshold)		$V_{PG(3.3VIN)}$	3.3VOUT falling	2.7		3	V
		$V_{PG(AUXIN)}$	AUX_{OUT} falling	2.7		3	
		$V_{PG(1.5VIN)}$	$1.5V_{OUT}$ falling	1.2		1.35	
PERST Assertion Delay From Output Voltage		$t_{FD(\overline{PERST})}$	$3.3V_{OUT}$, AUX_{OUT}, or $1.5V_{OUT}$ falling			500	ns
PERST De-assertion Delay From Output Voltage		$t_{RD(\overline{PERST})}$	$3.3V_{OUT}$, AUXOUT, and $1.5V_{OUT}$ rising within tolerance	4	10	20	ms
PERST Assertion Delay From SYSRST		$t_{FD2(\overline{PERST})}$	Max time from SYSRST asserted or de-asserted			500	ns
PERST Minimum Pulse Width		$t_{W(\overline{PERST})}$	$3.3V_{OUT}$, AUX_{OUT}, or $1.5V_{OUT}$ falling out of tolerance or triggered by SYSRST	100	250		μs
PERST Output Low Voltage		$V_{OL(\overline{PERST})}$	$I_{O(PERST)}$=500μA			0.4	V
PERST Output High Voltage		$V_{OH(\overline{PERST})}$		2.4			V
OC Output Low Voltage		$V_{OL(\overline{OC})}$	$I_{O(/OC)}$=2mA			0.4	V
OC Leakage Current		$I_{IKG(\overline{OC})}$	$V_{O(/OC)}$=3.6V			1	μA
OC Deglitch		$t_{D(\overline{OC})}$	Falling into or out of an overcurrent condition	6		20	mS
UNDERVOLTAGE LOCKOUT (UVLO)							
$3.3V_{IN}$ UVLO		$V_{UVLO(3.3VIN)}$	$3.3V_{IN}$ level, below which $3.3V_{IN}$ and $1.5V_{IN}$ switches are off	2.6		2.9	V
$1.5V_{IN}$ UVLO		$V_{UVLO(1.5VIN)}$	$1.5V_{IN}$ level, below which $3.3V_{IN}$ and $1.5V_{IN}$ switches are off	1		1.25	
AUX_{IN} UVLO		$V_{UVLO(AUXIN)}$	AUX_{IN} level, below which all switches are off	2.6		2.9	
UVLO Hysteresis		ΔV_{UVLO}			100		mV

Note: Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately. ELECTRICAL CHARACTERISTICS(Cont.)

■ SWITCHING CHARACTERISTICS

T_J=25°C, $V_{I(3.3VIN)}$=$V_{I(AUXIN)}$=3.3V, $V_{I(1.5VIN)}$=1.5V, $V_{I(/SHDNx)}$, $V_{I(/STBYx)}$=3.3V, $V_{I(/CPPEx)}$=$V_{I(/CPUSBx)}$=0V, $V_{I(/SYSRST)}$=3.3V, $\overline{\text{OCx}}$ and RCLKENx and $\overline{\text{PERSTx}}$ are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Rise Times	$3.3V_{IN}$ to $3.3V_{OUT}$	t_r	$C_{L(3.3VOUT)}$=0.1µF, $I_{O(3.3VOUT)}$=0A	0.1		3	ms
	AUX_{IN} to AUX_{OUT}		$C_{L(AUXOUT)}$=0.1µF, $I_{O(AUXOUT)}$=0A	0.1		3	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=0.1µF, $I_{O(1.5VOUT)}$=0A	0.1		3	
	$3.3V_{IN}$ to $3.3V_{OUT}$		$C_{L(3.3VOUT)}$=100µF, R_L=$V_{I(3.3VIN)}$/1A	0.1		6	
	AUX_{IN} to AUX_{OUT}		$C_{L(AUXOUT)}$=100µF, R_L=$V_{I(AUXIN)}$/0.250A	0.1		6	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=100µF, R_L=$V_{I(1.5VIN)}$/0.500A	0.1		6	
Output Fall Times When Card Removed (Both $\overline{\text{CPUSB}}$ And $\overline{\text{CPPE}}$ De-asserted)	$3.3V_{IN}$ to $3.3V_{OUT}$	t_f	$C_{L(3.3VOUT)}$=0.1µF, $I_{O(3.3VOUT)}$=0A	10		150	µs
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=0.1µF, $I_{O(AUXOUT)}$=0A	10		150	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=0.1µF, $I_{O(1.5VOUT)}$=0A	10		150	
	$3.3V_{IN}$ to $3.3V_{OUT}$		$C_{L(3.3VOUT)}$=20µF, $I_{O(3.3VOUT)}$=0A	2		30	ms
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=20µF, $I_{O(AUXOUT)}$=0A	2		30	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=20µF, $I_{O(1.5VOUT)}$=0A	2		30	
Output Fall Times When $\overline{\text{SHDN}}$ Asserted (Card Is Present)	$3.3V_{IN}$ to $3.3V_{OUT}$	t_f	$C_{L(3.3VOUT)}$=0.1µF, $I_{O(3.3VOUT)}$=0A	10		150	µs
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=0.1µF, $I_{O(AUXOUT)}$=0A	10		150	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=0.1µF, $I_{O(1.5VOUT)}$=0A	10		150	
	$3.3V_{IN}$ to $3.3V_{OUT}$		$C_{L(3.3VOUT)}$=100µF, R_L=$V_{I(3.3VIN)}$/1A	0.1		5	ms
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=100µF, R_L=$V_{I(AUXIN)}$/0.250A	0.1		5	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=100µF, R_L=$V_{I(1.5VIN)}$/0.500A	0.1		5	
Turn-On Propagation Delay	$3.3VI_N$ to $3.3V_{OUT}$	$t_{pd(on)}$	$C_{L(3.3VOUT)}$=0.1µF, $I_{O(3.3VOUT)}$=0A	0.1		1	ms
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=0.1µF, $I_{O(AUXOUT)}$=0A	0.05		0.5	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=0.1µF, $I_{O(1.5VOUT)}$=0A	0.1		1	
	$3.3V_{IN}$ to $3.3V_{OUT}$		$C_{L(3.3VOUT)}$=100µF, R_L=$V_{I(3.3VIN)}$/1A	0.1		1.5	
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=100µF, R_L=$V_{I(AUXIN)}$/0.250A	0.05		1	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=100µF, R_L=$V_{I(1.5VIN)}$/0.500A	0.1		1.5	
Turn-Off Propagation Delay	$3.3V_{IN}$ to $3.3V_{OUT}$	$t_{pd(off)}$	$C_{L(3.3VOUT)}$=0.1µF, $I_{O(3.3VOUT)}$=0A	0.1		1.5	ms
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=0.1µF, $I_{O(AUXOUT)}$=0A	0.05		0.5	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=0.1µF, $I_{O(1.5VOUT)}$=0A	0.1		1.5	
	$3.3V_{IN}$ to $3.3V_{OUT}$		$C_{L(3.3VOUT)}$=100µF, R_L=$V_{I(3.3VIN)}$/1A	0.1		1.5	
	AUX_{IN} to $VAUX_{OUT}$		$C_{L(AUXOUT)}$=100µF, R_L=$V_{I(AUXIN)}$/0.250A	0.05		0.5	
	$1.5V_{IN}$ to $1.5V_{OUT}$		$C_{L(1.5VOUT)}$=100µF, R_L=$V_{I(1.5VIN)}$/0.500A	0.1		1	

■ FUNCTIONAL TRUTH TABLES

Table 1. Truth Table for Voltage Outputs

VOLTAGE INPUTS (Note 1)			LOGIC INPUTS			VOLTAGE OUTPUTS (Note 2)			MODE (Note 3)
AUX_{IN}	$3.3V_{IN}$	$1.5V_{IN}$	$\overline{SHDN}$	$\overline{STBY}$	$\overline{CP}$ (Note 4)	AUX_{OUT}	$3.3V_{OUT}$	$1.5V_{OUT}$	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

Notes: 1. For input voltages, On means the respective input voltage is higher than its turnon threshold voltage; otherwise, the voltage is Off (for AUX input, Off means the voltage is close to zero volt.)

2. For output voltages, On means the respective power switch is turned on so the input voltage is connected to the output; Off means the power switch and its output discharge FET are both off; GND means the power switch is off but the output discharge FET is on so the voltage on the output is pulled down to 0V.

3. Mode assigns each set of input conditions and respective output voltage results to a different name. These modes are referred to as input conditions in the following Truth Table for Logic Outputs.

4. $\overline{CP}$ = $\overline{CPUSB}$ and $\overline{CPPE}$ -equal to 1 when both $\overline{CPUSB}$ and $\overline{CPPE}$ signals are logic high, or equal to 0 when either $\overline{CPUSB}$ or $\overline{CPPE}$ is low.

Table 2. Truth Table for Logic Outputs

INPUT CONDITIONS			LOGIC OUTPUTS	
MODE	$\overline{SYSRST}$	RCLKEN (Note 1)	$\overline{PERST}$	RCLKEN (Note 2)
OFF	X	X	0	0
Shutdown				
No Card				
Standby				
Card Inserted	0	Hi-Z	0	1
	0	0	0	0
	1	Hi-Z	1	1
	1	0	0	0

Notes: 1. RCLKEN as a logic input in this column. RCLKEN is an I/O pin and it can be driven low externally, left open, or connected to high-impedance terminals, such as the gate of a MOSFET. It must not be driven high externally.

2. RCLKEN as a logic output in this column.

■ POWER STATES

OFF mode

If AUX_{IN} is not present, then all input-to-output power switches are kept off (OFF mode).

Shutdown mode

If AUX_{IN} is present and $\overline{SHDN}$ is asserted (logic low), then all input-to-output power switches are kept off and the output discharge FETs are turned on (Shutdown mode). If $\overline{SHDN}$ is asserted and then de-asserted, the state on the outputs is restored to the state prior to $\overline{SHDN}$ assertion.

No Card mode

If $3.3V_{IN}$, AUX_{IN} and $1.5V_{IN}$ are present at the input of the power switch and no card is inserted, then all input-to-output power switches are kept off and the output discharge FETs are turned on (No Card mode).

Card Inserted mode

If $3.3V_{IN}$, AUX_{IN} and $1.5V_{IN}$ are present at the input of the power switch prior to a card being inserted, then all input-to-output power switches are turned on once a card-present signal ($\overline{CPUSB}$ and/or $\overline{CPPE}$) is detected (Card Inserted mode).

Standby mode

If a card is present and all output voltages are being applied, then the $\overline{STBY}$ is asserted (logic low); the AUX_{OUT} voltage is provided to the card, and the $3.3V_{OUT}$ and $1.5V_{OUT}$ switches are turned off (Standby mode).

If a card is present and all output voltages are being applied, then the $1.5V_{IN}$, or $3.3V_{IN}$ is removed from the input of the power switch; the AUX_{OUT} voltage is provided to the card and the $3.3V_{OUT}$ and $1.5V_{OUT}$ switches are turned off (Standby mode).

If prior to the insertion of a card, the AUX_{IN} is available at the input of the power switch and $3.3V_{IN}$ and/or $1.5V_{IN}$ are not, or if $\overline{STBY}$ is asserted (logic low), then no power is made available to the card (OFF mode). If $1.5V_{IN}$ and $3.3V_{IN}$ are made available at the input of the power switch after the card is inserted and $\overline{STBY}$ is not asserted, all the output voltages are made available to the card (Card Inserted mode).

■ DISCHARGE FETs

The discharge FETs on the outputs are activated whenever the device detects that a card is not present (No Card mode). Activation occurs after the input-to-output power switches are turned off (break before make). The discharge FETs de-activate if either of the card-present lines go active low, unless the $\overline{SHDN}$ pin is asserted.

The discharge FETs are also activated whenever the $\overline{SHDN}$ input is asserted and stay asserted until $\overline{SHDN}$ is de-asserted.

■ APPLICATION INFORMATION

Introduction to ExpressCard™

An ExpressCard module is an add-in card with a serial interface based on PCI Express and/or Universal Serial Bus (USB) technologies. An ExpressCard™ comes in two form factors defined as ExpressCard|34 or ExpressCard|54. The difference, as defined by the name, is the width of the module, 34mm or 54mm, respectively. Host systems supporting the ExpressCard™ module can support either the ExpressCard|34 or ExpressCard|54 or both.

ExpressCard™ Power Requirements

Regardless of which ExpressCard™ module is used, the power requirements as defined in the ExpressCard™ Standard apply to both on an individual slot basis. The host system is required to supply 3.3V, 1.5V, and AUX to each of the ExpressCard™ slots. However, the voltage is only applied after an ExpressCard™ is inserted into the slot.

The ExpressCard™ connector has two pins, $\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$, which are used to signal the host when a card is inserted. If the ExpressCard™ module itself connects the $\overline{\text{CPPE}}$ to ground, the logic low level on that signal indicates to the host that a card supporting PCI Express has been inserted. If $\overline{\text{CPUSB}}$ is connected to ground, then the ExpressCard™ module supports the USB interface. If both PCI Express and USB are supported by the ExpressCard™ module, then both signals, $\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$, must be connected to ground.

In addition to the Card Present signals ($\overline{\text{CPPE}}$ and $\overline{\text{CPUSB}}$), the host system determines when to apply power to the ExpressCard™ module based on the state of the system. The state of the system is defined by the state of the 3.3 V, 1.5V, and AUX input voltage rails. For the sake of simplicity, the 3.3V and 1.5V rails are defined as the primary voltage rails as oppose to the auxiliary voltage rail, AUX.

ExpressCard™ Power Switch Operation

The ExpressCard power switch resides on the host, and its main function is to control when to send power to the ExpressCard™ slot. The ExpressCard™ power switch makes decisions based on the Card Present inputs and on the state of the host system as defined by the primary and auxiliary voltage rails.

The following conditions define the operation of the host power controller:

1. When both primary power and auxiliary power at the input of the ExpressCard™ power switch are off, then all power to the ExpressCard™ connector is off regardless of whether a card is present.

2. When both primary power and auxiliary power at the input of the ExpressCard™ power switch are on, then power is only applied to the ExpressCard™ after the ExpressCard™ power switch detects that a card is present.

3. When primary power (either +3.3V or +1.5V) at the input of the ExpressCard™ power switch is off and auxiliary power at the input of the ExpressCard™ power switch is on, then the ExpressCard™ power switch behaves in the following manner:

(a) If neither of the Card Present inputs is detected (no card inserted), then no power is applied to the ExpressCard™ slot.

(b) If the card is inserted after the system has entered this power state, then no power is applied to the ExpressCard™ slot.

(c) If the card is inserted prior to the removal of the primary power (either +3.3V or +1.5V or both) at the input of the ExpressCard™ power switch, then only the primary power (both +3.3V and +1.5V) is removed and the auxiliary power is sent to the ExpressCard™ slot.

Figure 2 through Figure 7 illustrate the timing relationships between power/logic inputs and outputs of ExpressCard™.

■ TEST CIRCUITS AND VOLTAGE WAVEFORMS

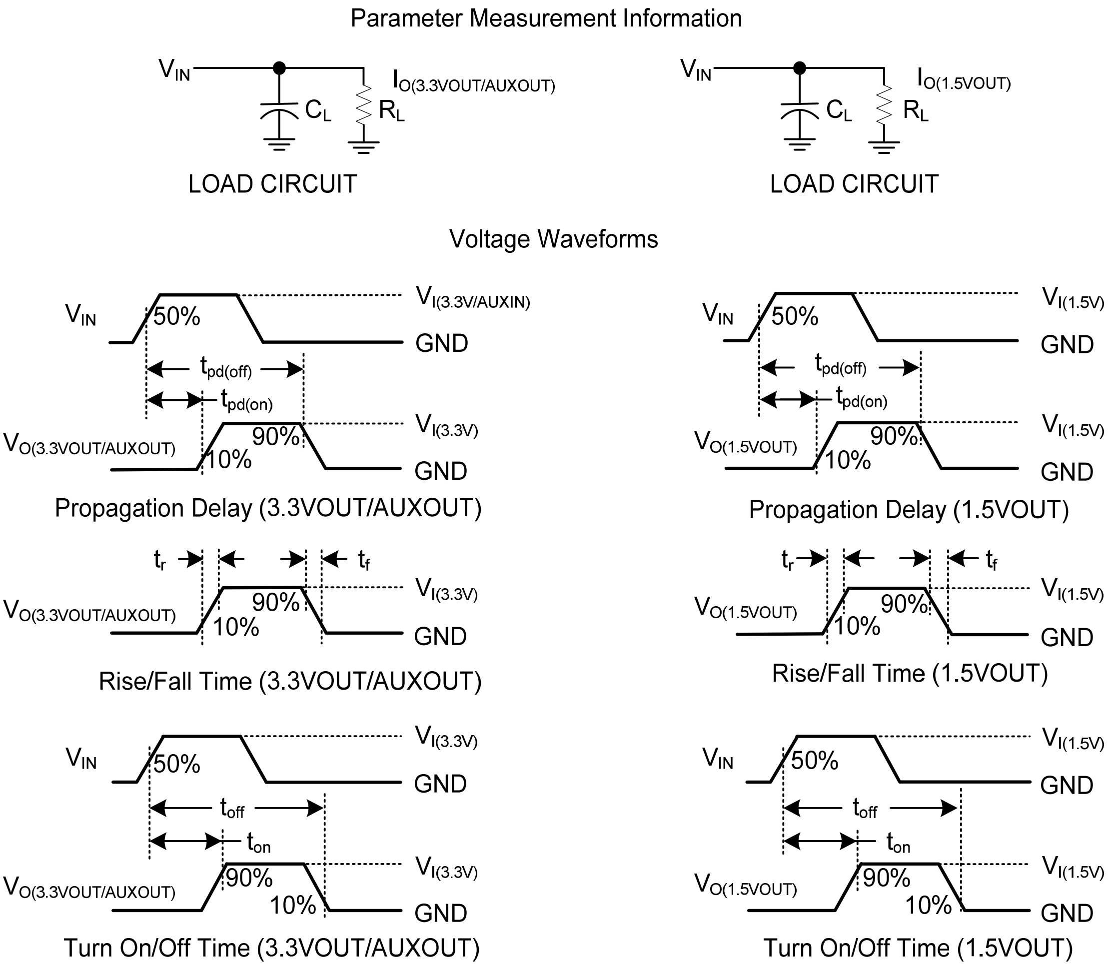
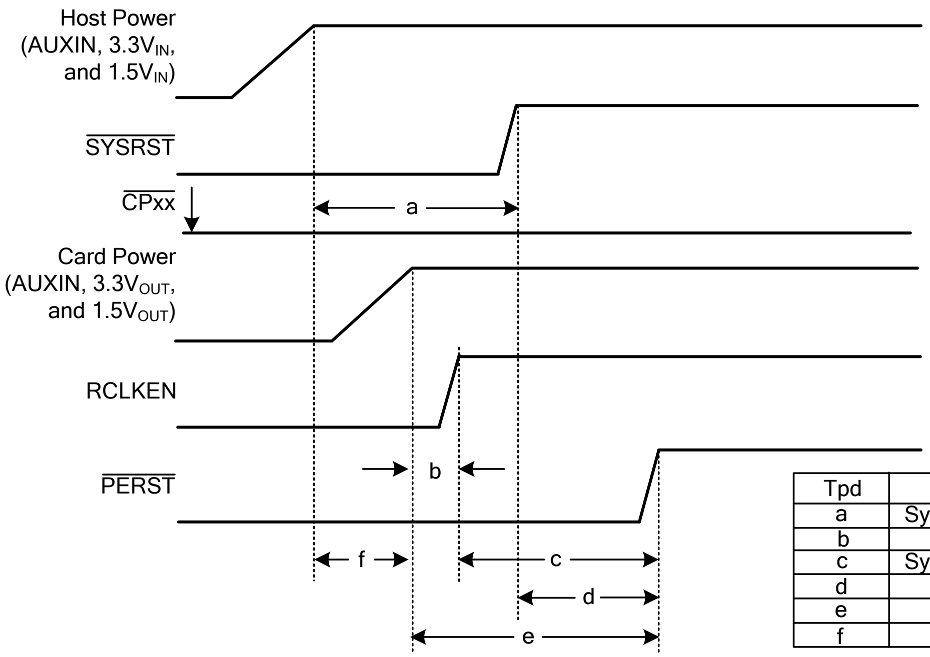


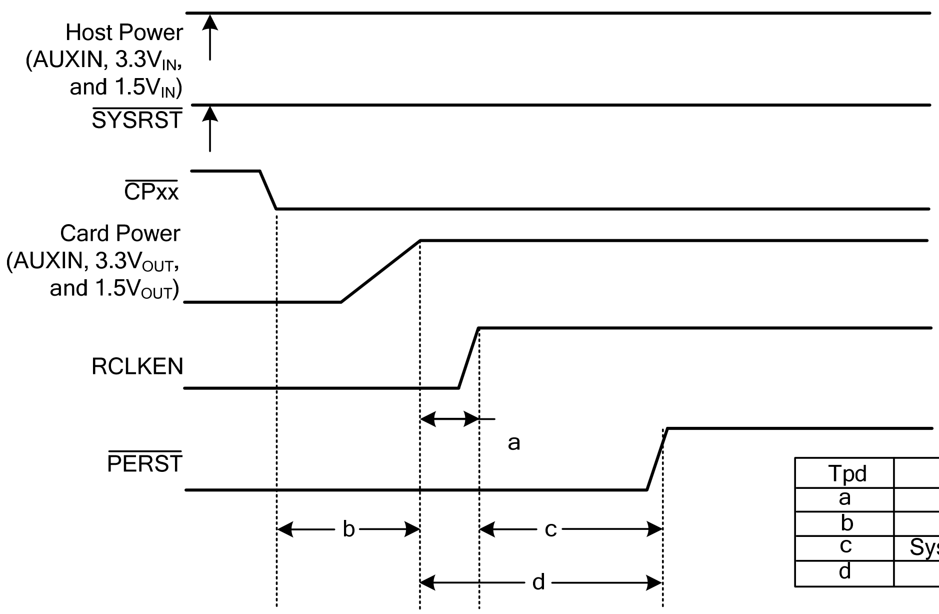
Figure 1. Test Circuits and Voltage Waveforms

■ EXPRESS CARD TIMING DIAGRAMS



Tpd	Min	Max	Units
a	System Dependent		
b		100	µs
c	System Dependent		
d	100		µs
e	4	20	ms
f		10	ms

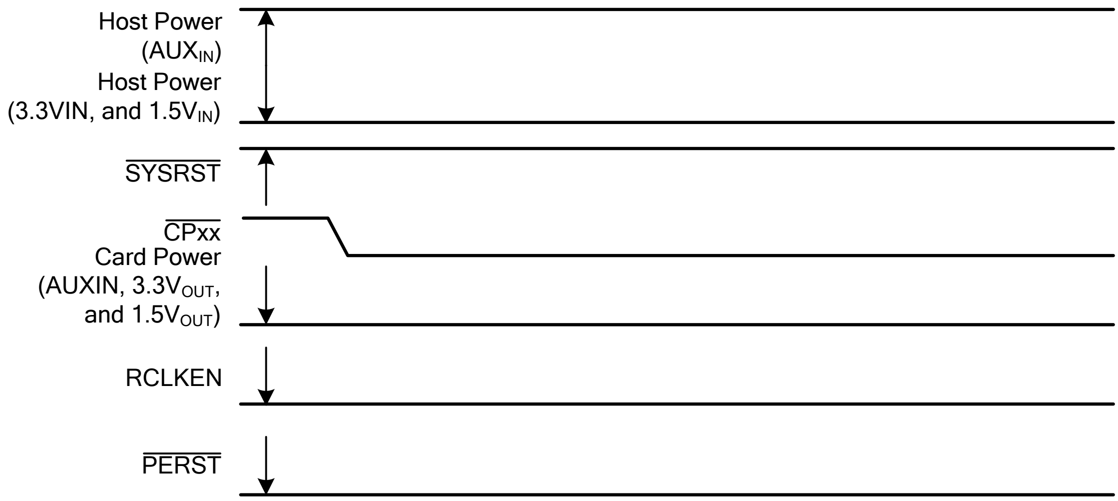
Figure 2. Timing Signals - Card Present Before Host Power Is On



Tpd	Min	Max	Units
a		100	µs
b		10	ms
c	System Dependent		
d	4	20	ms

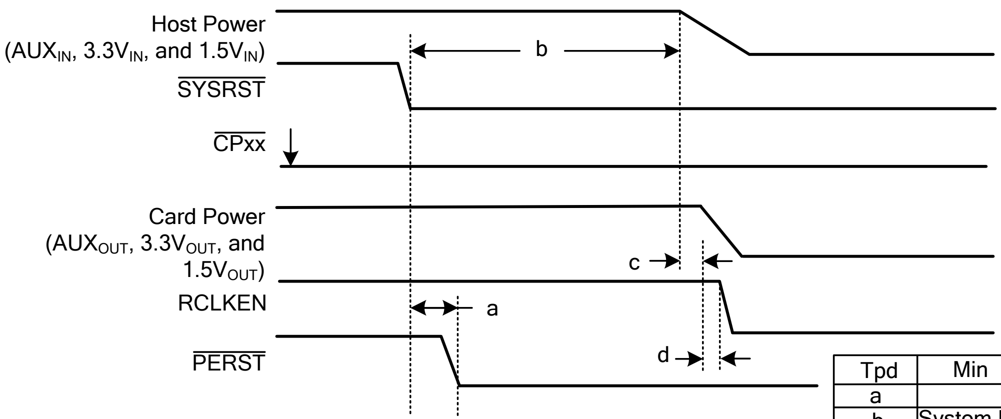
Figure 3. Timing Signals - Host Power Is On Prior Card Insertion

■ EXPRESS CARD TIMING DIAGRAMS(Cont.)



Note: Once 3.3V and 1.5V are applied, the power switch follows the power-up sequence of Figure 2 or Figure 3.

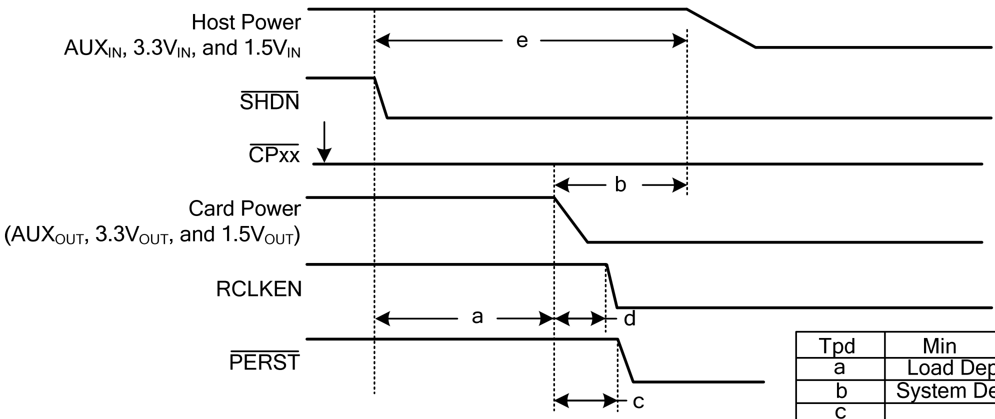
Figure 4. Timing Signals - Host System In Standby Prior to Card Insertion



Tpd	Min	Max	Units
a		500	ns
b	System Dependent		
c	Load Dependent		
d		500	ns

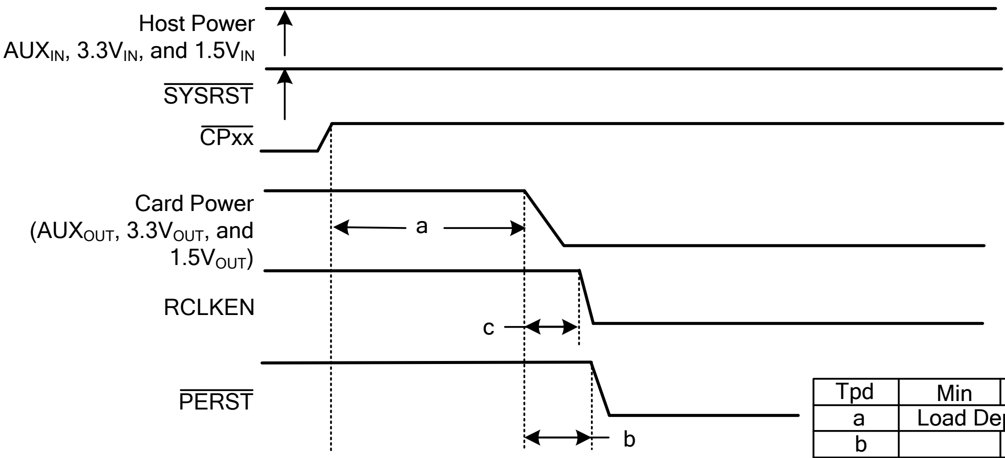
Figure 5. Timing Signals - Host - Controlled Power Down

■ EXPRESS CARD TIMING DIAGRAMS(Cont.)



Tpd	Min	Max	Units
a	Load Dependent		
b	System Dependent		
c		500	ns
d		500	ns
e	System Dependent		

Figure 6. Timing Signals - Controlled Power Down When SHDN Asserted



Tpd	Min	Max	Units
a	Load Dependent		
b		500	ns
c		500	ns

Figure 7. Timing Signals - Surprise Card Removal

■ TYPICAL APPLICATION CIRCUIT