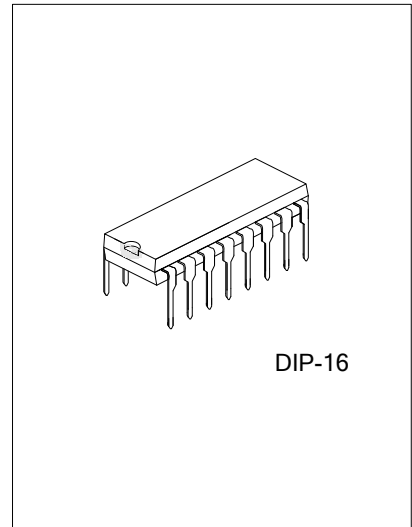




### ELECTRONIC PROTECTION ARRAY FOR ESD AND OVER-VOLTAGE PROTECTION



#### DESCRIPTION

The UTC **USP720** is an electronic protection array, it uses UTC's advanced technology to provide customers with high peak current capability, high switching speed, high ESD interface capability for HBM standards, low input leakage current and low input capacitance, etc.

The UTC **USP720** is suitable for ESD and OVP to sensitive input circuits.

#### FEATURES

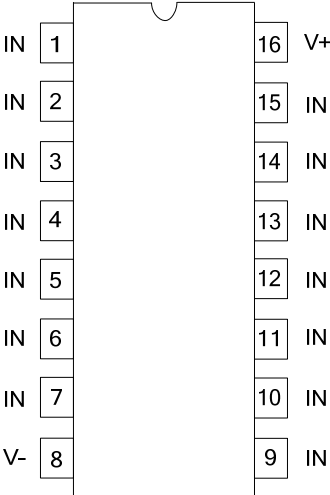
- \* High peak current capability
- \* High switching speed
- \* High ESD interface capability for HBM standards
- \* Low input leakage current
- \* Low input capacitance

#### ORDERING INFORMATION

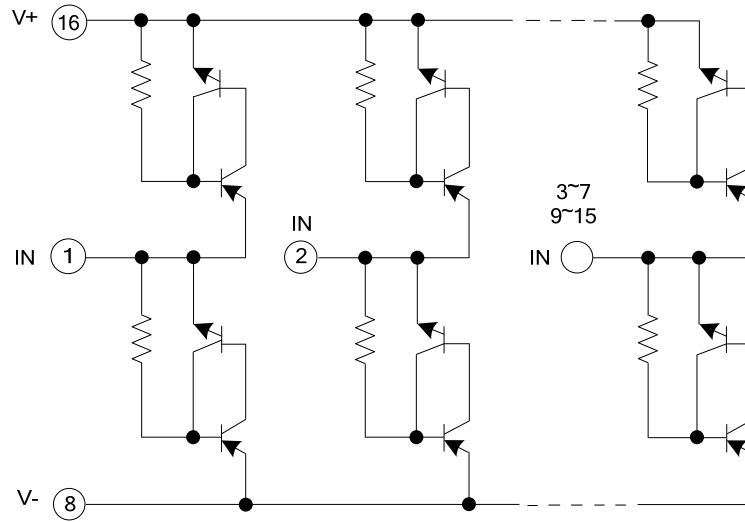
| Ordering Number |               | Package | Packing |
|-----------------|---------------|---------|---------|
| Lead Free       | Halogen Free  |         |         |
| USP720L-D16-T   | USP720G-D16-T | DIP-16  | Tube    |

|                   |   |  |
|-------------------|---|--|
| USP720G-D16-T<br> | (1)Packing Type<br>(2)Package Type<br>(3)Halogen Free | (1) T: Tube<br>(2) D16 : DIP-16<br>(3) G: Halogen Free, L: Lead Free |
|-------------------|---|--|

■ PIN CONFIGURATION



■ FUNCTIONAL BLOCK DIAGRAM



### ■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER  | SYMBOL    | RATINGS  | UNIT        |
|--|-----------|----------|-------------|
| Continuous Supply Voltage, (V+) - (V-)                 | $V_S$     | 35       | V           |
| Forward Peak Current, $I_{IN}$ to VCC, $I_{IN}$ to GND | $I_F$     | $\pm 2$  | A           |
| Storage Temperature                                    | $T_{STG}$ | -65~+150 | $^{\circ}C$ |
| Operating Junction Temperature                         | $T_J$     | 150      | $^{\circ}C$ |
| Load Dump and Reverse Battery (Note 2)                 |           |          |             |

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the UTC USP720 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01 $\mu$ F or larger from the V+ and V- pins to ground are recommended.

### ■ THERMAL CHARACTERISTICS

| PARAMETER           | SYMBOL        | RATINGS | UNIT          |
|---------------------|---------------|---------|---------------|
| Junction to Ambient | $\theta_{JA}$ | 90      | $^{\circ}C/W$ |

Notes:  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### ■ ELECTRICAL CHARACTERISTICS ( $T_A = -40^{\circ}C \sim 105^{\circ}C$ ; $V_{IN} = 0.5V_{CC}$ , unless otherwise specified.)

| PARAMETER   | SYMBOL          | TEST CONDITIONS            | MIN | TYP | MAX | UNIT     |
|---|-----------------|----------------------------|-----|-----|-----|----------|
| Operating Voltage Range, $V_{SUPPLY} = [(V+) - (V-)]$ | $V_{SUPPLY}$    |                            | 2   |     | 30  | V        |
| Forward Voltage Drop:                                 | IN to V-        | $I_{IN} = 1A$ (Peak Pulse) |     | 2   |     | V        |
|   | IN to V+        |                            |     | 2   |     | V        |
| Input Leakage Current                                 | $I_{IN}$        |                            | -20 | 5   | 20  | nA       |
| Quiescent Supply Current                              | $I_{QUIESCENT}$ |                            |     | 50  | 200 | nA       |
| Equivalent SCR ON Threshold                           |                 |                            |     | 1.1 |     | V        |
| Equivalent SCR ON Resistance                          |                 | $V_{FWD}/I_{FWD}$          |     | 1   |     | $\Omega$ |
| Input Capacitance                                     | $C_{IN}$        |                            |     | 3   |     | pF       |
| Input Switching Speed                                 | $t_{ON}$        |                            |     | 2   |     | ns       |

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