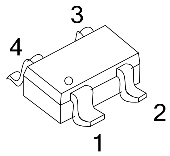
4-PIN µP VOLTAGE MONITORS WITH MANUAL RESET INPUT



SOT-143

■ DESCRIPTION

The UTC **83CXXX** is a microprocessor supervisory circuit. It has an active-low $\overline{\text{RESET}}$ and push-pull outputs. The circuit can assert a reset signal as long as the V_{CC} power supplies voltage dropping below a preset threshold and it keep the reset signal for at least 140ms when V_{CC} has risen above the reset threshold. The reset threshold can be operated with multi-supply voltages.

The UTC **83CXXX** provides the circuit with perfect reliability and low cost through eliminating external components and adjustments when applied with +5V, +3.3V, +3.0V power supply The UTC **83CXXX** also provide a de-bounced manual reset input.

The reset comparator can work despite of fast transients on V_{CC}, and the outputs are guaranteed to be in the right logic state while V_{CC} is down to 1V.

In applications, the UTC **83CXXX** is suitable for computers, intelligent instruments, controllers, critical microprocessor and microcomputer power monitors, portable or battery-powered equipment, automotive.

■ FEATURES

* +3V, +3.3V, and +5V power-supply voltages
* Full temperature rated
* Supply current: 5µA
* Available in configuration: push-pull $\overline{\text{RESET}}$ output
* 140ms minimum power-on reset pulse width
* Guaranteed reset to V_{CC} = +1V
* Power supply transient Immunity
* Eliminating external components
* Manual reset input

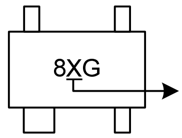
■ ORDERING INFORMATION

Ordering Number	Package	Packing
83CXXXG-AD4-R	SOT-143	Tape Reel

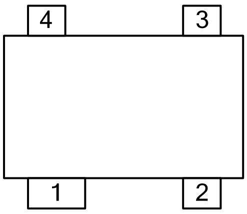
Note: XXX: Output Voltage, refer to Marking Information.

83CXXXG-AD4-R	
(1) Packing Type	(1) R: Tape Reel
(2) Package Type	(2) AD4: SOT-143
(3) Green Package	(3) G: Halogen Free and Lead Free
(4) Output Voltage Code	(4) XXX: Refer to Marking Information

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-143	B: 2.93V C: 3.08V	

■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION
1	GND	Ground
2	$\overline{RESET}$	$\overline{RESET}$ output remains low while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
3	$\overline{MR}$	Manual reset input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted as long as $\overline{MR}$ is low and for at least 140ms after $\overline{MR}$ returns high, This active-low input has an internal 20kΩ pull-up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused.
4	V_{CC}	Supply voltage (+5V, +3.3V, +3.0V)

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Terminal Voltage (respect to GND)		V_{CC}	-0.3 ~ +6.0	V
$\overline{\text{RESET}}$ Voltage	Push-Pull	$V_{\overline{RESET}}$	-0.3 ~ (V_{CC}+0.3)	V
$\overline{\text{RESET}}$ Voltage	Open Drain	$V_{\overline{RESET}}$	-0.3 ~ +6.0	V
Input Current		I_{CC}	20	mA
Output Current ($\overline{\text{RESET}}$)		I_{OUT}	20	mA
Power Dissipation (Ta =+70°C)		P_D	320	mW
Derated Above 70°C		P_D	4	mW/°C
Operating Temperature		T_{OPR}	-40~+105	°C
Storage Temperature		T_{STG}	-65~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = full range, T_A =-40°C~+105°C. Typical values are at T_A=25°C, unless otherwise specified)

83C293 (2.93V) (V_{CC}= 3.3V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} Range		V_{CC}	T_A=0°C~+70°C	1.0		5.5	V
V_{CC} Range		V_{CC}	T_A=-40°C~+105°C	1.2		5.5	V
$\overline{\text{MR}}$ Input Threshold		V_{IH}	V_{CC}>$V_{TH(MAX)}$	1.98			V
$\overline{\text{MR}}$ Input Threshold		V_{IL}	V_{CC}>$V_{TH(MAX)}$			0.825	V
Reset Threshold		V_{TH}	T_A=25°C	2.871	2.93	2.988	V
Supply Current		I_{CC}	V_{CC}<3.6V, T_A=-40°C~+105°C		5	8	μA
$\overline{\text{RESET}}$ Output Current (push-pull active low)	Low	I_{OL}	V_{CC}=2.5V, $V_{\overline{RESET}}$ = 0.5V	8			mA
$\overline{\text{RESET}}$ Output Current (push-pull active low)	High	I_{OH}	V_{CC}= 3.3V, $V_{\overline{RESET}}$ = 2.8V	3			mA
$\overline{\text{MR}}$ Pull-up Resistance				10	20	30	kΩ
Reset Threshold Tempco					70		ppm/°C
V_{CC} to Reset Delay			V_{CC}= V_{TH}~(V_{TH}-100mV)		15		
Reset Active Timeout Period			V_{CC}= $V_{TH(MAX)}$	140	310	520	ms
$\overline{\text{MR}}$ Minima Pulse Width		t_{MR}			10		μs
$\overline{\text{MR}}$ Glitch Immunity (Note)					100		ns
$\overline{\text{MR}}$ to Reset Propagation Delay		t_{MD}			0.5		μs

83C308 (3.08V) (V_{CC}=3.3V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} Range		V_{CC}	T_A=0°C~+70°C	1.0		5.5	V
V_{CC} Range		V_{CC}	T_A=-40°C~+105°C	1.2		5.5	V
$\overline{\text{MR}}$ Input Threshold		V_{IH}	V_{CC}>$V_{TH(MAX)}$	1.98			V
$\overline{\text{MR}}$ Input Threshold		V_{IL}	V_{CC}>$V_{TH(MAX)}$			0.825	V
Reset Threshold		V_{TH}	T_A=25°C	3.018	3.08	3.141	V
Supply Current		I_{CC}	V_{CC}<3.6V, T_A=-40°C~+105°C		5	8	μA
$\overline{\text{RESET}}$ Output Current (push-pull active low)	Low	I_{OL}	V_{CC}=2.5V, $V_{\overline{RESET}}$ = 0.5V	8			mA
$\overline{\text{RESET}}$ Output Current (push-pull active low)	High	I_{OH}	V_{CC}= 3.3V, $V_{\overline{RESET}}$ = 2.8V	3			mA
$\overline{\text{MR}}$ Pull-up Resistance				10	20	30	kΩ
Reset Threshold Tempco					70		ppm/°C
V_{CC} to Reset Delay			V_{CC}= V_{TH} ~ (V_{TH}-100mV)		15		
Reset Active Timeout Period			V_{CC}= $V_{TH(MAX)}$	140	310	520	ms
$\overline{\text{MR}}$ Minima Pulse Width		t_{MR}			10		μs
$\overline{\text{MR}}$ Glitch Immunity (Note)					100		ns
$\overline{\text{MR}}$ to Reset Propagation Delay		t_{MD}			0.5		μs

Note: "Glitches" of 100ns or less typical values will not generate a reset pulse.

■ DETAILED DESCRIPTION

The UTC **83CXXX** have a push-pull output stage. A microprocessor's (µP's) reset input initiates the microprocessor in a known state. The UTC **83CXXX** assert a reset signal as long as the V_{CC} power supply voltage drops below a preset threshold. When V_{CC} has risen over the reset threshold, the devices keep the signal for at least 140ms. They have a function of preventing code-execution errors during power-up, power-down, or brownout conditions by resetting.

See the manual reset input section if you want to see function that the manual reset input ($\overline{MR}$) can initiate a reset.

Manual Reset Input

Many products based on microprocessor need manual reset characteristic, allowing them to initiate a reset. Reset keeps working while $\overline{MR}$ is low, and when $\overline{MR}$ returns high it is for the reset Active Timeout Period (t_{RP}). TTL or CMOS-logic levels, or with open-drain / collector outputs both can drive $\overline{MR}$. $\overline{MR}$ will be started by a logic low on manual reset .Because the input has a build-in 20kΩ pull-up resistor; it can be left open if it is not used. We can put a 0.1µF capacitor from $\overline{MR}$ to ground if $\overline{MR}$ is driven from long cables or the device is used in a noisy environment strengthening additional noise capacity. Connecting a normally open momentary switch from $\overline{MR}$ to ground to create a manual-reset function, and external debounce circuitry is not required.

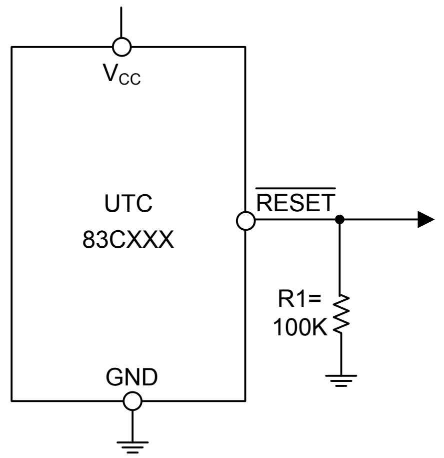


Figure 1. $\overline{RESET}$ Valid to V_{CC} = Ground Circuit

■ APPLICATION INFORMATION

1. Ensuring a Valid Reset Output Down to V_{CC} = 0

The UTC **83CXXX** $\overline{RESET}$ output no more sinks current when V_{CC} drops below 1V—it becomes an open circuit. Therefore, high-impedance CMOS logic input connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications since most microprocessors and other circuitry can't be operated when V_{CC} is under 1V. In figure 1, however, in applications where $\overline{RESET}$ must be valid down to 0V. In order to causes any stray leakage currents to flow to ground, adding a pull-down resistor to $\overline{RESET}$, that holding $\overline{RESET}$ low. (R1's value is not critical and the value 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground).

2. Benefits of Highly Accurate Reset Threshold

Most microprocessor supervisor ICs has reset threshold voltages between 5% and 10% below the value of nominal supply voltages. If using ICs rated at only the nominal supply ±5%, this leaves an uncertainty zone where the supply is between 5% and 10% low and where the reset may or may not be asserted.

The UTC 83C308 with high accuracy ensure that the reset is asserted closely to 5% limit and long before the supply has declined to 10% below nominal.

■ TYPICAL APPLICATION CIRCUIT