UNISONIC TECHNOLOGIES CO., LTD

82XX

Preliminary

LINEAR INTEGRATED CIRCUIT

MONOLITHIC IC 82XX SERIES

DESCRIPTION

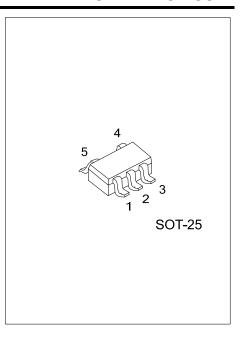
The normal operation of the UTC **82XX** is that while the power is turned on or interrupted, detect power supply voltage and then reset the system accurately.

The internal circuits of the UTC **82XX** include a built-in fixed delay time generating circuit. With a counter timer using an analog/digital hybrid circuit, the UTC **82XX** as new low reset type system reset ICs expands the delay time series.

These ICs can be used in a variety of CPU systems and other logic systems.

■ FEATURES

- * Internal Fixed Delay Time Setting by Counter Timer
- * Grate Delay Time Temperature Characteristics: ±800ppm/°C
- * Operating Limit Voltage as 0.65V(Typ.)
- * Hysteresis Voltage Provided: 50mV(Typ.)
- * Circuit Current While On Iccl=300µA(Typ.)
- * Circuit Current While Off ICCH=200µA(Typ.)

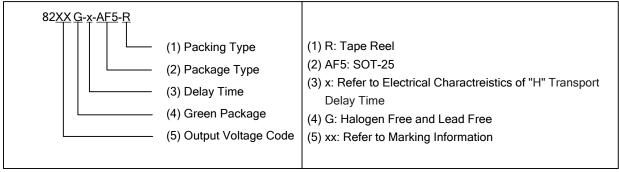


■ ORDERING INFORMATION

Ordering Number	Package	Packing
82XXG-x-AF5-R	SOT-25	Tape Reel

Notes: xx: Output Voltage, refer to Marking Information.

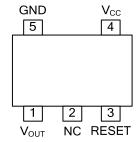
x: Delay Time, refer to Electrical Characteristics of "H" Transport Delay Time



■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-25	25:2.5V 27:2.7V 2K:2.93V	Voltage Code

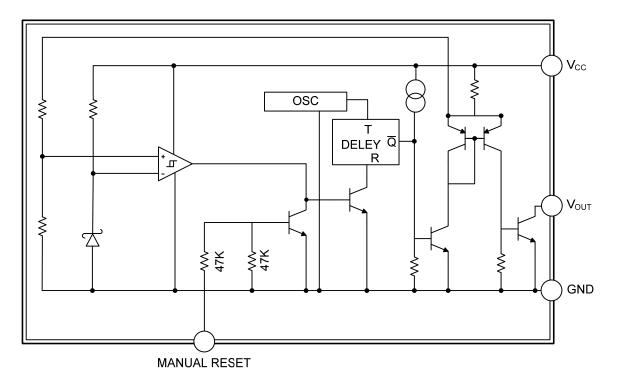
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{OUT}	Output pin
2	NC	Connected nothing
3	RESET	Reset control pin
4	V _{cc}	Supply voltage
5	GND	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V _{cc}	-0.3~+10	V
Manual Reset Input Voltage	V_{RESET}	-0.3~+10	V
Power Dissipation	P_{D}	400	mW
Operating Temperature	T_{OPR}	-20~+75	°C
Storage Temperature	T _{STG}	-40~+125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **ELECTRICAL CHARACTERISTICS** (T_A=25°C, Unless otherwise specified)

V_S=2.5V~2.93V

PAF	PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Detection Voltage		Vs	$V_{OL} \le 0.4V$, $V_{CC} = H \rightarrow L$, $R_L = 470\Omega$ (See Test Circuit 1)		V _S -0.15V	Vs	V _S +0.15V	V	
Low-Level Output Voltage		V _{OL}	$V_{CC}=V_{S(min)}$ -0.05V, R_L =470 Ω (See Test Circuit 1)		0.1	0.4	٧		
Operating Pow	er Supply Vo	ltage	V _{OPL}	R _L =4.7kΩ, V _{OL} ≤0.4V		0.65	0.85	V	
Hysteresis Voltage		ΔVs	V _{CC} =L→H→L , R _L =470Ω (See Test Circuit 1)	30	50	100	mV		
Detection Voltage Temperature Coefficient		$\frac{V_S}{\Delta T}$	R _L =470Ω, T _A =-20°C~+75°C (See Test Circuit 1)		±0.01		%/°C		
Output Leakage Current		I _{OH}	V _{CC} =10V (See Test Circuit 1)				±0.1	μΑ	
Circuit Current		On	I _{CCL}	V _{CC} = V _{S(MIN)} -0.05V, R _L =∞			300	600	μΑ
(See Test Circu	uit 1)	Off	I _{CCH}	V _{CC} =V _{S(TYP)} /0.85V, R _L =∞			200	350	μΑ
	"H" Transport Delay Time		t _{РLН}		Р	30	50	75	mS
				R_L =4.7 $K\Omega$, C_L =100PF (Note 1) (See Test Circuit 2)	Q	60	100	150	mS
"H" Transport [R	120	200	300	mS
					S	240	400	600	mS
					Т	480	800	1200	mS
"L" Transport Delay Time		t _{PHL}	R_L =4.7k Ω , C_L =100PF (Note 1) (See Test Circuit 2)			10		μS	
Output Current While on 1		I _{OL1}	V_{CC} =VS min0.05V, R _L =0Ω (See Test Circuit 1)		8			mA	
Output Current While on 2		I _{OL2}	T_A =-20°C ~+75°C, R_L =0 Ω (Note 2) (See Test Circuit 1)		6			mA	
Pin Reset	Input High \	/oltage	V_{RESH}			2.0			V
	Input High (Current	I _{RESH}	V _{RESET} =2V			80	μΑ	
	Input Low V	oltage	V_{RESL}					0.8	V

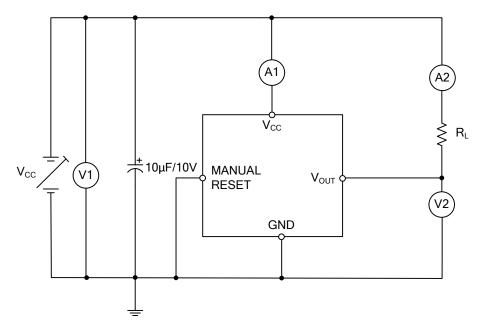
Notes: 1. t_{PLH} : V_{CC} = $(V_{S(TYP)}$ -0.4V) \rightarrow $(V_{S(TYP)}$ +0.4V)

 $t_{PHL} : V_{CC} = (V_{S(TYP)} + 0.4V) \rightarrow (V_{S(TYP)} - 0.4V)$

- 2. V_{CC} = $V_{S(MIN)}$ -0.15V
- 3. $\ensuremath{V_{\text{OUT}}}$ pin is low when manual reset pin is high.

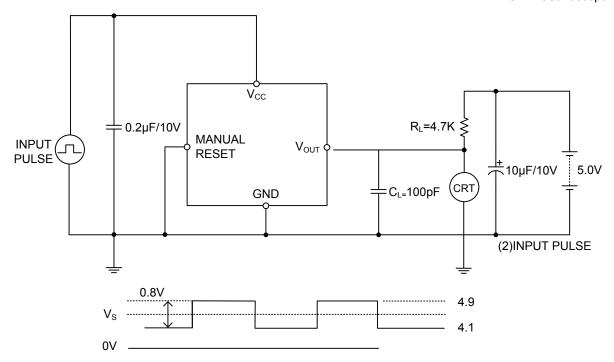
V_{OUT} pin is high when manual reset pin is low.

■ TEST CIRCUITS



Test Circuit 1

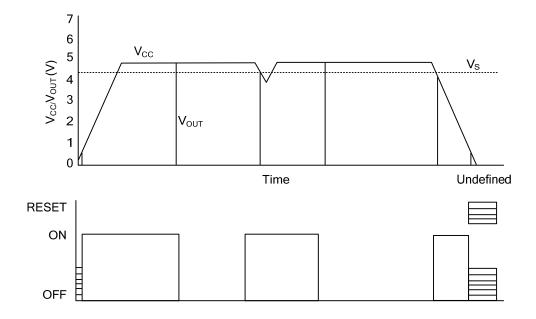
A: DC ammeter V: DC voltmeter CRT: Oscilloscope



Note Input model is an example for 82XX

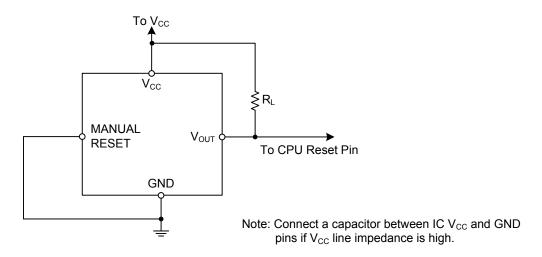
Test Circuit 2

■ TIMING CHART

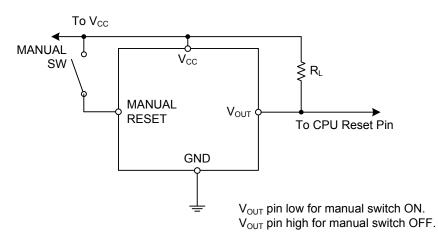


■ TYPICAL APPLICATION CIRCUITS

1. Normal hard reset

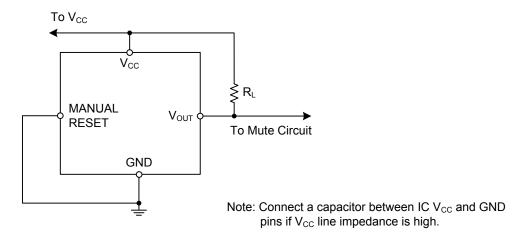


2. Manual reset



Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.

3. Mute circuit



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