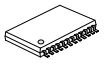
L16B06

CMOS IC

16-BIT CONSTANT CURRENT LED DRIVER



SSOP-24 (209mil)

■ DESCRIPTION

The **L16B06** is a constant-current sink driver specifically designed for LED display applications. The device incorporates shift registers, data latches, and constant current circuitry on the silicon CMOS chip. The maximum output current value of all 16 channels is adjustable by a single external resistor.

■ FEATURES

*Constant-current outputs: 3mA to 60mA adjustable by one external resistor
*Maximum output voltage: 17V
*Maximum clock frequency: 25MHz
*Power supply voltage: 3.3V to 5V
*In-rush current control
*Bit-to-bit skew: ±3% Chip-to-chip skew: ±6%
*Package and pin assignment compatible to conventional LED drivers

■ APPLICATIONS

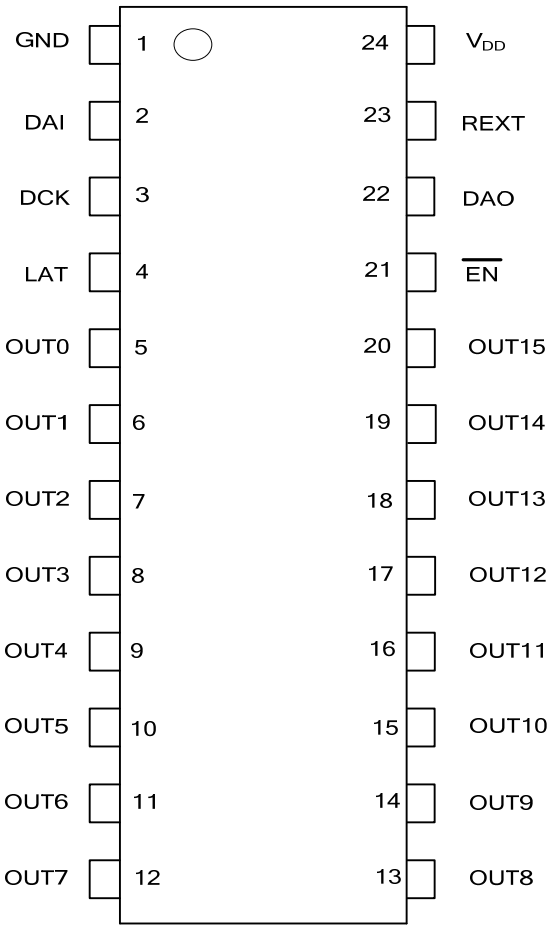
*Indoor/Outdoor LED Video Display
*LED Variable Message Signs (VMS) System

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L16B06L-R24-T	L16B06G-R24-T	SSOP-24	Tube
L16B06L-R24-R	L16B06G-R24-R	SSOP-24	Tape Reel

L16B06L-R24-T (1) Packing Type (2) Package Type (3) Lead Free	(1) T: Tube, R: Tape Reel (2) R24: SSOP-24 (3) L: Lead Free, G: Halogen Free

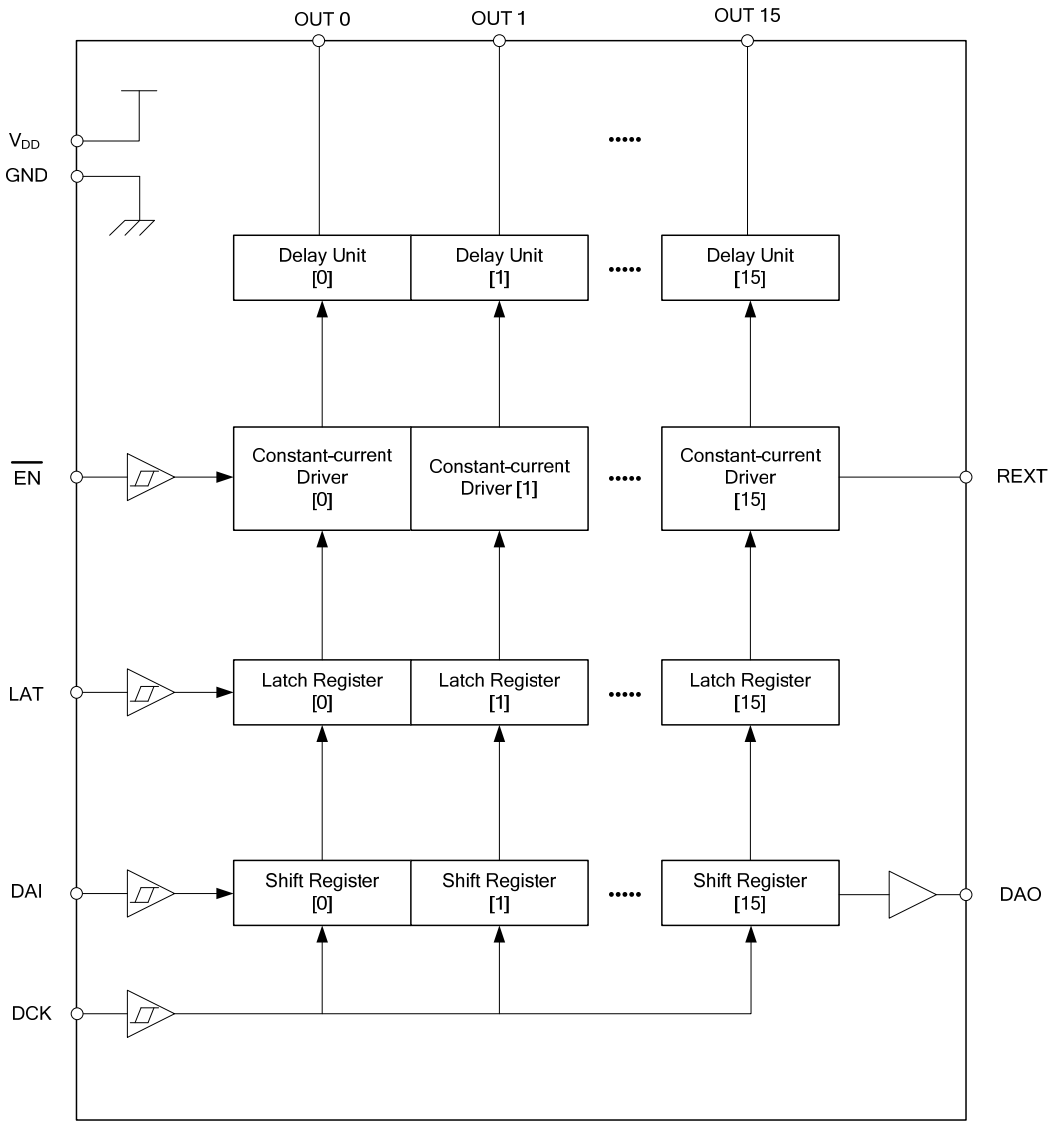
■ PIN CONNECTION



■ PIN DESCRIPTION

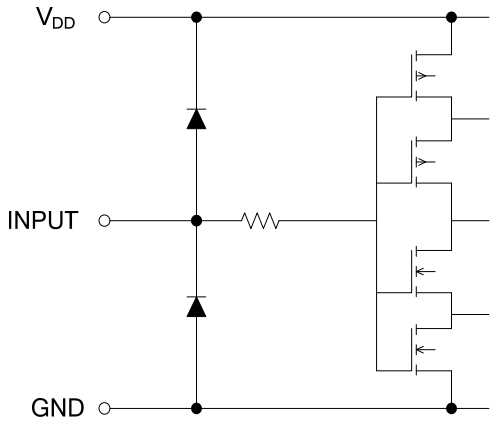
PIN No.	PIN NAME	FUNCTION
1	GND	Ground terminal.
2	DAI	Serial data input terminal.
3	DCK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of DCK.
4	LAT	Input terminal of data strobe. Data on shift register goes through at the high level of LAT (level trigger). Otherwise, data is latched.
5-20	OUT0-15	Sink constant-current outputs (open-drain).
21	$\overline{EN}$	Output enable terminal: 'H' for all outputs are turned off, 'L' for all outputs are active.
22	DAO	Serial data output terminal.
23	REXT	External resistors connected between REXT and GND for output current value setting.
24	V_{DD}	Supply voltage terminal.

■ BLOCK DIAGRAM

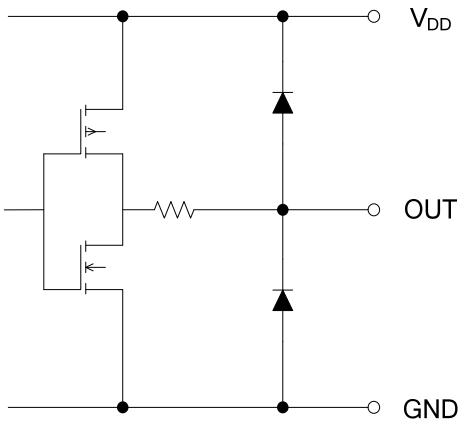


■ EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

1. DCK, DAI, LAT, $\overline{EN}$ TERMINALS



2. DAO TERMINALS



■ MAXIMUM RATINGS (T_A=25°C, T_J=150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ~ 7.0	V
Input Voltage	V_{IN}	-0.3 ~ VDD+0.3	V
Output Current	I_{OUT}	70	mA
Output Voltage	V_{OUT}	-0.3 ~ 17	V
Input Clock Frequency	F_{DCK}	25	MHz
Operating Temperature	T_{OPR}	-40 ~ 85	°C
Storage Temperature	T_{STG}	-55 ~ 150	°C

■ RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		3.3	5.0	5.5	V
Output Voltage	V_{OUT}	Driver On	1.0		$0.5xV_{DD}$	V
Output Voltage	V_{OUT}	Driver Off			17	V
Output Current	I_O	OUTn	5		60	mA
Input Voltage	V_{IH}	V_{DD}=3.3V ~ 5.5V	$0.8xV_{DD}$		V_{DD}	V
	V_{IL}		0.0		$0.2x_{VDD}$	

■ ELECTRICAL CHARACTERISTICS (V_{DD}=5.0 V, T_A=25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage “H” Level	V_{IH}	CMOS logic level	$0.8×V_{DD}$		V_{DD}	V
Input Voltage “L” Level	V_{IL}	CMOS logics2 level	GND		$0.2×V_{DD}$	V
Output Leakage Current	I_{OL}	V_{OH}=17V			±1	μA
Output Voltage (DAO)	V_{OL}	I_{OL}=1.5mA			0.2	V
	V_{OH}	I_{OH}=1.4mA	V_{DD}-0.2			V
Output Current Skew (Channel-to-Channel)	I_{OL1}	V_{OUT}=1.0V, R_{REXT}=2.2KΩ			±3	%
Output Current Skew (Chip-to-Chip)	I_{OL2}				±6	%
Output Voltage Regulation	% / V_{OUT}	R_{REXT} =2.2KΩ, V_{OUT}=1V ~ 3V		±0.1	±0.5	%/V
Supply Voltage Regulation	% / V_{DD}	R_{REXT} =2.2KΩ		±1	±4	

■ ELECTRICAL CHARACTERISTICS(Cont.)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Current	$I_{DD(OFF)}$	power on all pins are open unless V_{DD} and GND		3	4	mA
	$I_{DD(OFF)}$	input signal is static Rrext=2.9KΩall outputs turn off		5	6	mA
	$I_{DD(ON)}$	input signal is static Rrext=2.9KΩall outputs turn on		5	6	mA
	$I_{DD(OFF)}$	input signal is static Rrext=1.05KΩall outputs turn off		9	10	mA
	$I_{DD(ON)}$	input signal is static Rrext=1.05KΩall outputs turn on		9	10	mA

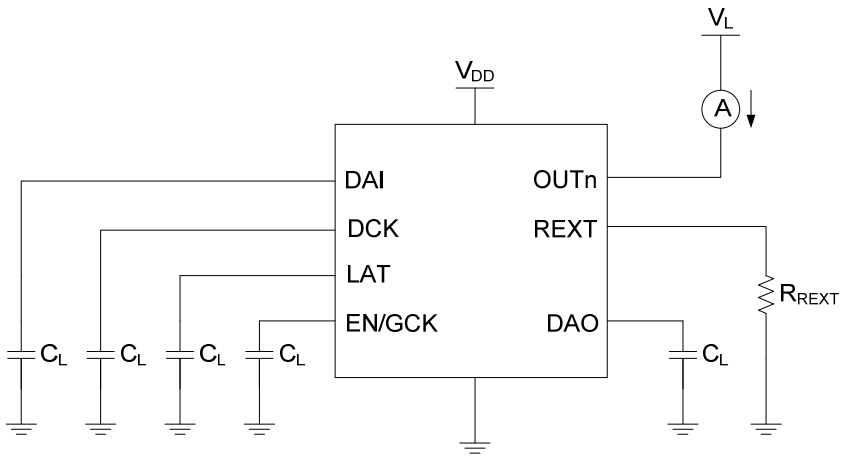
■ SWITCHING CHARACTERISTICS (V_{DD}=5.0V, T_A=25°C, unless otherwise specified)

CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Propagation Delay (‘L’ to ‘H’)	EN-to-OUT0	t_{PLH}	V_{IH}=V_{DD}, V_{IL}=GND R_{REXT}=2.2kΩ, V_L=5.0V, C_L=13pF		52		ns
	LAT-to-OUT0				49		ns
	DCK-to-DAO				20		ns
Propagation Delay (‘H’ to ‘L’)	EN-to-OUT0	t_{PHL}			22		ns
	LAT-to-OUT0				75		ns
	DCK-to-DAO				19.5		ns
Output Current Rise Time		t_{OR}			33.5		ns
Output Current Fall Time		t_{OF}			6		ns
Output Delay Time (OUT(n)-to-OUT(n+1))		t_{OD}			5		ns

■ SWITCHING CHARACTERISTICS (V_{DD}=3.3V, T_A=25°C, unless otherwise specified)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L’ to ‘H’)	EN-to-OUT0	t_{PLH}	V_{IH}=V_{DD}, V_{IL}=GND R_{REXT} =2.2KΩ V_L=5.0V, C_L=13pF		51		ns
	LAT-to-OUT0				21.5		ns
	DCK-to-DAO				12		ns
Propagation Delay (‘H’ to ‘L’)	EN-to-OUT0	t_{PHL}			23		ns
	LAT-to-OUT0				49		ns
	DCK-to-DAO				11.5		ns
Output Current Rise Time		t_{OR}			35		ns
Output Current Fall Time		t_{OF}			10		ns
Output Delay Time (OUT(n)-to-OUT(n+1))		t_{OD}			10		ns

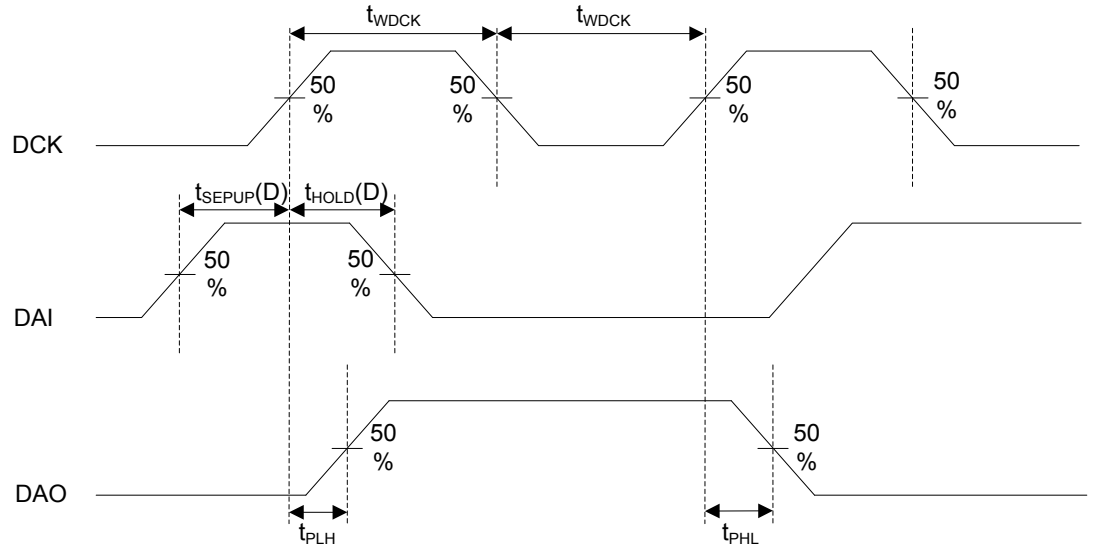
■ SWITCHING CHARACTERISTICS(Cont.)



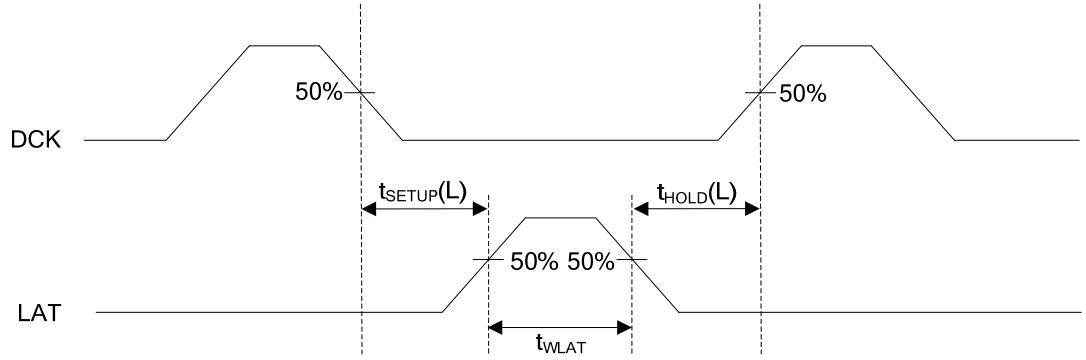
Switching Characteristics Test Circuit

■ TIMING DIAGRAM

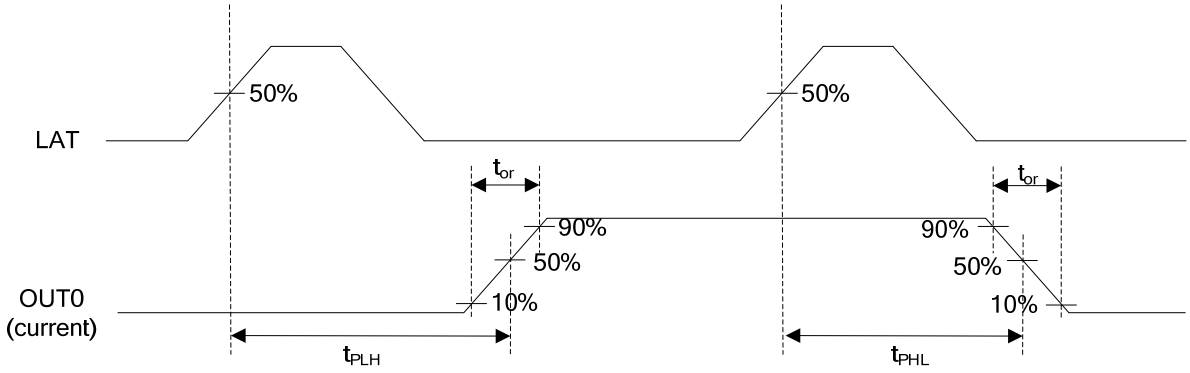
1. DCK-DAI, DAO



2. DCK-LAT

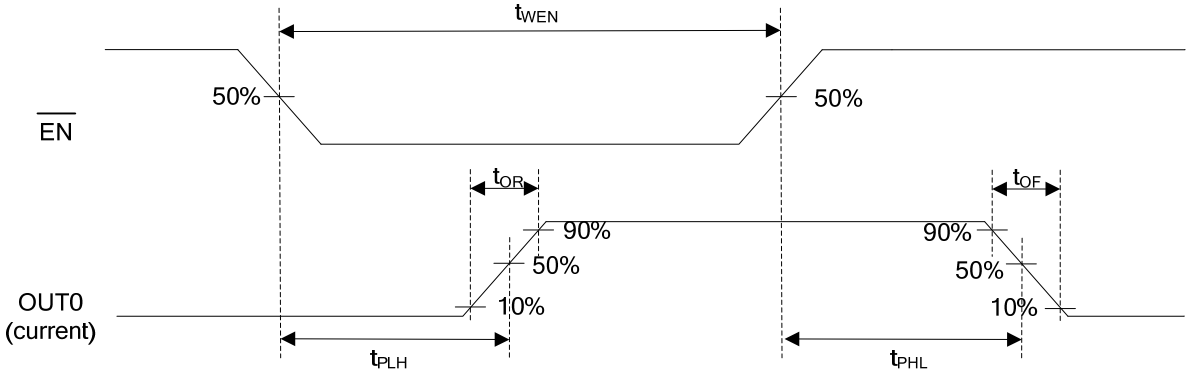


3. LAT-OUT0

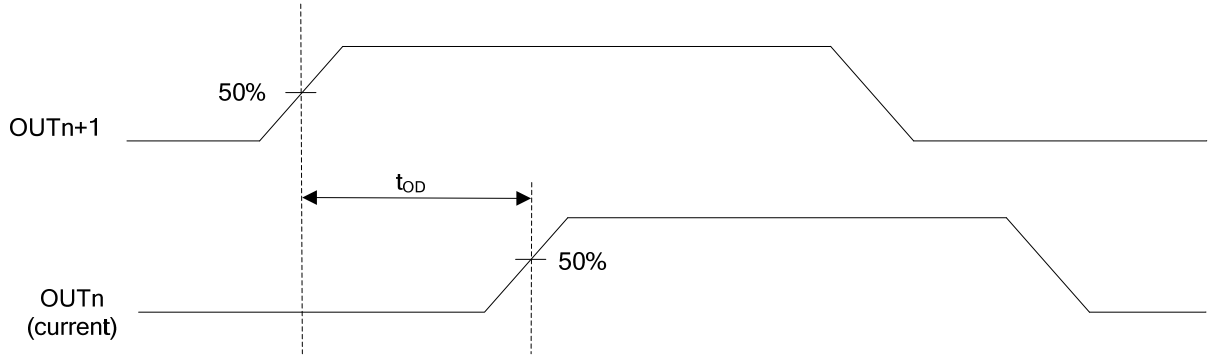


■ TIMING DIAGRAM(Cont.)

4. $\overline{EN}$ -OUT0



5. OUTn+1-OUTn



■ CONSTANT-CURRENT OUTPUT

Constant-current value of each output channel is set by an external resistor connected between the REXT pin an GND. Varying the resistor value can adjust the current scale ranging from 3mA to 60mA. The reference voltage of REXT terminal (Vrext) is approximately 1.2V. The output current value is calculated roughly by the following equation:

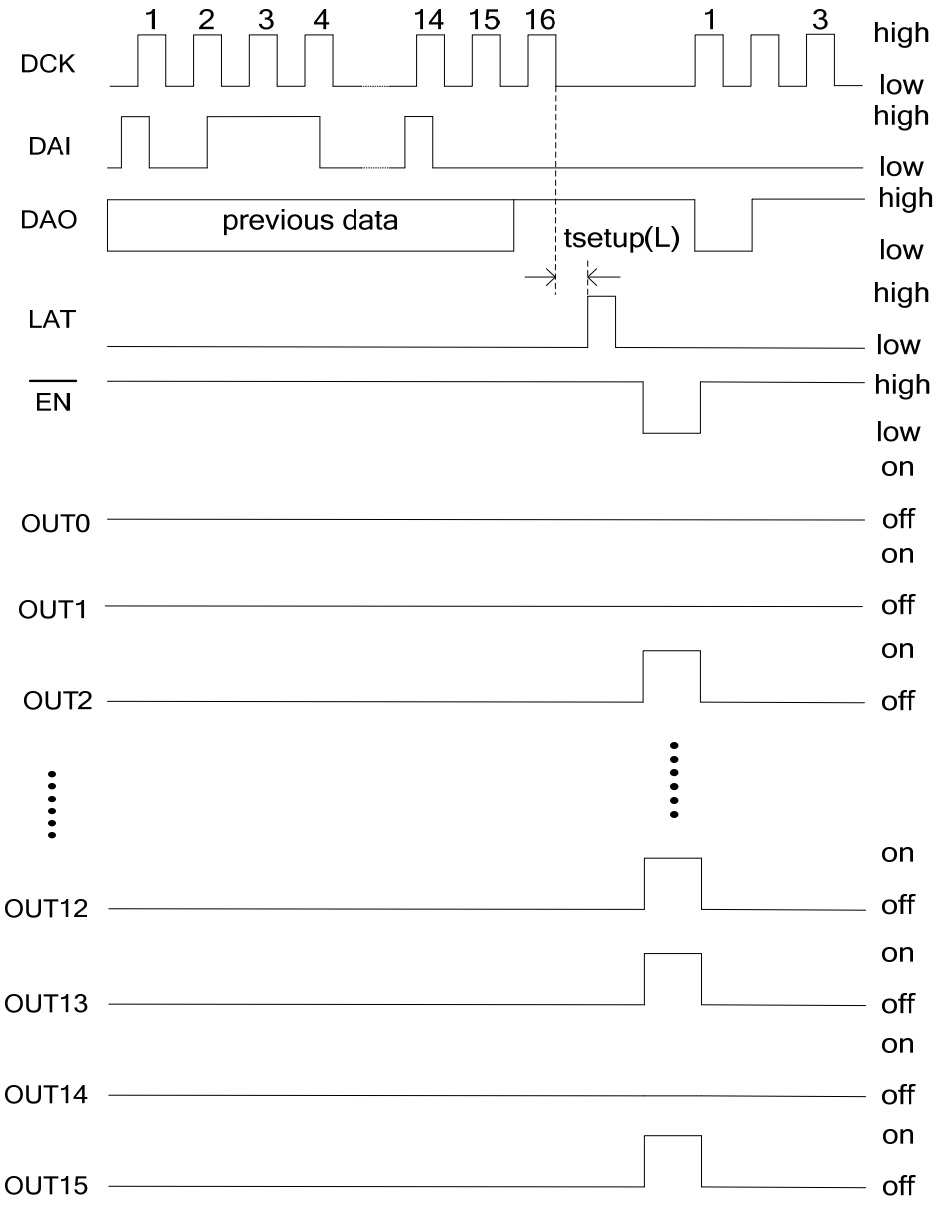
$$I_{OUT}(mA) \cong \frac{V_{REXT}(V)}{R_{REXT}(K\Omega)} \times M$$

Iout(mA)	3	5	10	20	30	40	50
M	55	54.1	50	46.6	45	43.3	41.6s

In order to obtain a good performance of constant-current output, a suitable output voltage is necessary.

■ SERIAL DATA INTERFACE

The serial-in data (DAI) will be clocked into 16 bit shift register synchronized on the rising edge of the clock (DCK). The data '1' represents the corresponding current output 'ON', while the data '0' stands for 'OFF'. The data will be transferred into the 16 bit latch register when the strobe signal (LAT) is 'H' (level trigger); otherwise, the data will be held. The trigger timing of the serial-out data (DAO) will be shifted out on synchronization to the rising edge of the clock. All outputs are turned off while enable terminal (EN) is kept at high level. And they are active when EN shifts to low.

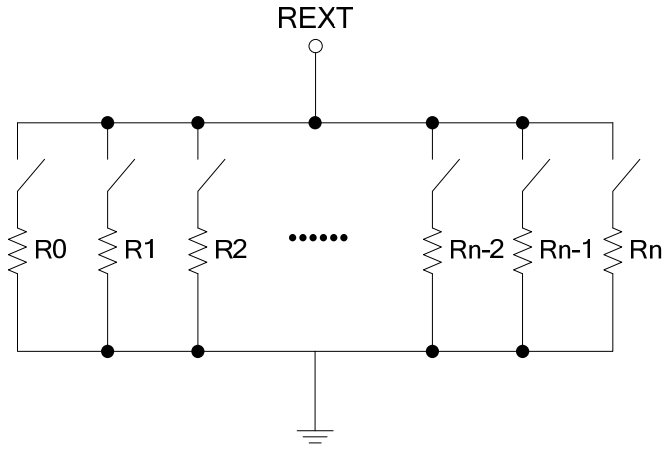


■ OUTPUTS DELAY

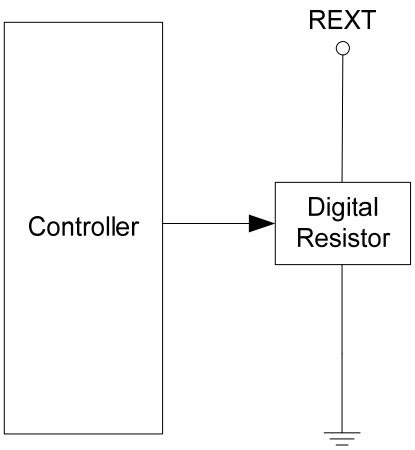
Large in-rush currents will occur when the system activates all the outputs at once. To reduce this effect, **L16B06** is designed to have a constant unit of delay (around 5ns) between outputs. The delay sequence for every output goes like this: OUT0 (no delay) → OUT15 → OUT1 → OUT14 → OUT2 → OUT13 → OUT3 → OUT12 → OUT4 → OUT11 → OUT5 → OUT10 → OUT6 → OUT9 → OUT7 → OUT8 (the largest delay).

■ GLOBAL BRIGHTNESS CONTROL

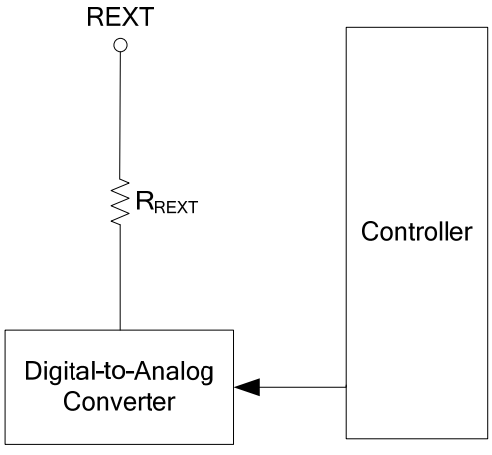
L16B06 has no built-in global brightness control feature. In order to obtain a lower resolution of global brightness control effect, two methods could be utilized. One is providing PWM signal synchronized on latch pulse to modulate the output enable terminal ($\overline{EN}$ pin). The other is to adjust the R_{REXT} value or voltage drop across the external resistor. Please see the reference circuit below:



Global Brightness Control with Resistor Ladder



Global Brightness Control with Digital Resistor



Global Brightness Control with D/A Converter

■ POWER DISSIPATION

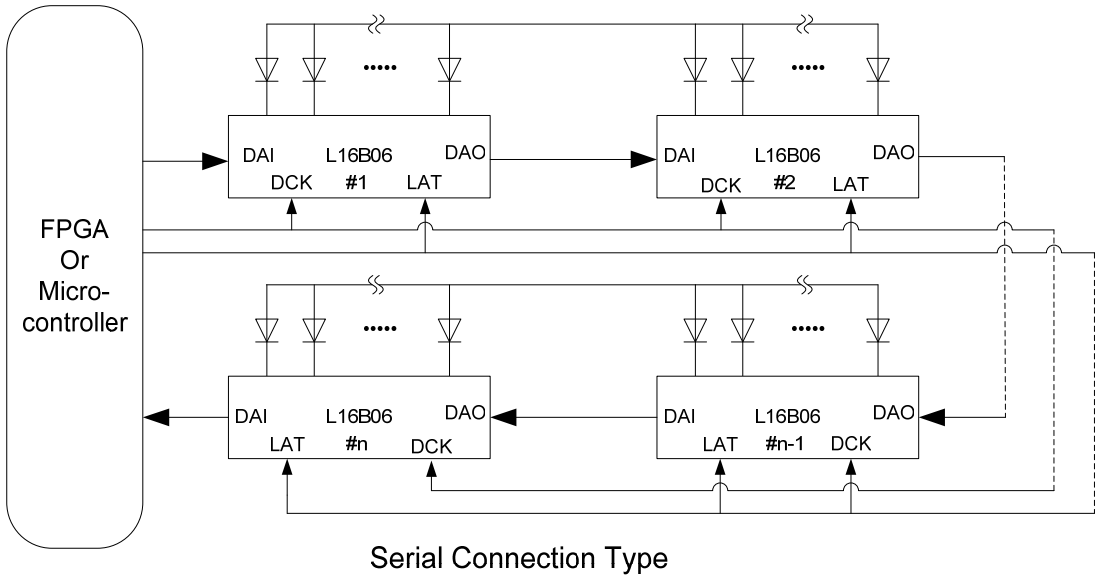
The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$P_D(max)(watt)= \frac{T_J\ (Junction\ temperature)(max)(°C) - T_A(Ambient\ Temperature)}{R_{TH}\ (Junction\ -\ to\ -\ air\ thermal\ resistance)(°C/watt)}$$

The power consumption of IC can be determined by the following equation an should be less than the maximum allowable power dissipation:

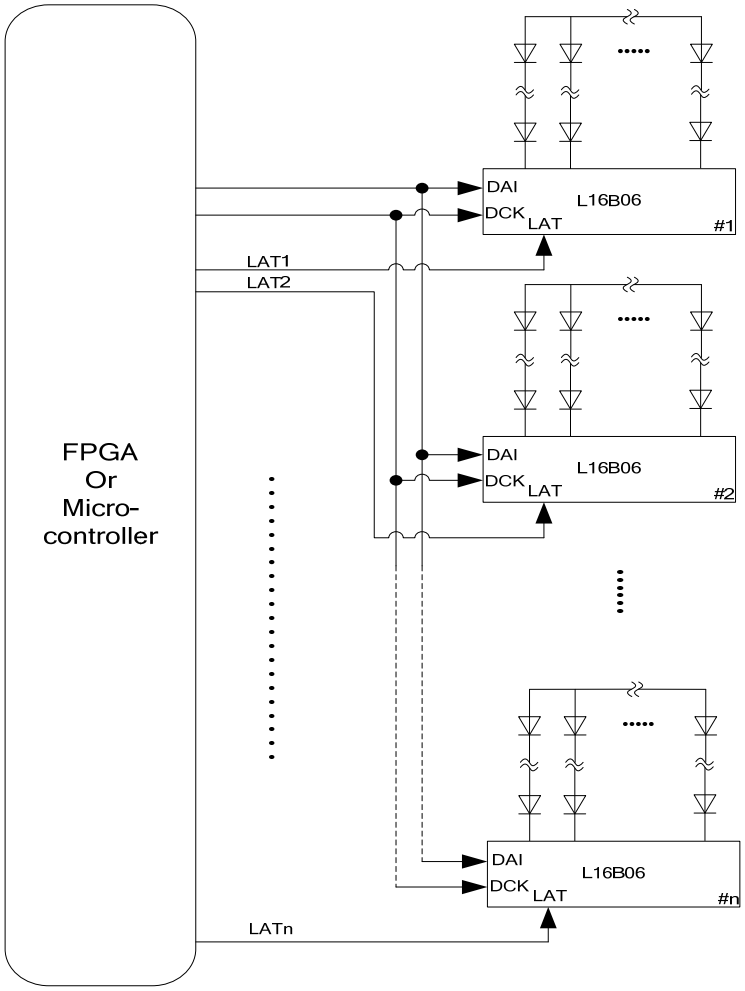
$$P_D(W) = V_{CC}(V) \times I_{DD}(A) + V_{OUT}\ 0 \times I_{OUT}\ 0 \times D_{UTY}\ 0 + ... + V_{OUT}\ 15 \times I_{OUT}\ 15 \times D_{UTY}\ 15 \le P_D\ (max)(W)$$

■ TYPICAL APPLICATION



Serial Connection Type

■ TYPICAL APPLICATION(Cont.)



Parallel Connection Type