

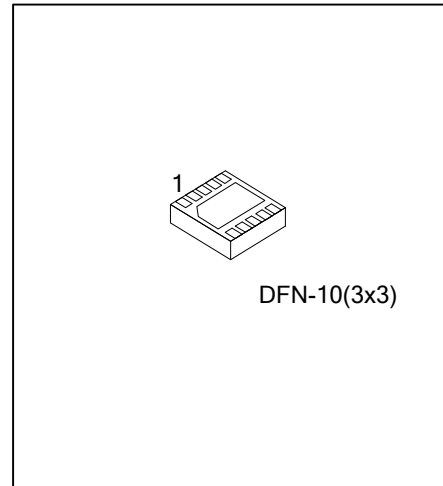


UD05301

Preliminary

LINEAR INTEGRATED CIRCUIT

6.0V, 3.5A, 1.2MHZ, HIGH EFFICIENCY PWM STEP-DOWN DC/DC CONVERTER



DESCRIPTION

UTC **UD05301** is a high efficiency step-down DC/DC converter operated with the current mode and the constant frequency. The internal switch and synchronous rectifier are integrated for high efficiency. UTC **UD05301** can supply 3.5A of load current from 2.7V ~ 5.5V supply voltage.

The switching frequency is set at 1.2MHz, allowing the use of small surface mount inductors and capacitors. It can run 100% duty cycle for low dropout application. UTC **UD05301** is available in a DFN3X3-10 package.

FEATURES

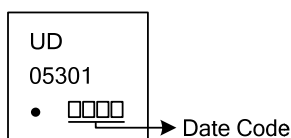
- * 2.7V~5.5V Input Voltage Range
- * High Efficiency: Up to 95%
- * 1.2MHz Constant Switching Frequency
- * 3.5A Available Load Current
- * 100% Duty Cycle in Dropout
- * Current Mode Control
- * Short Circuit Protection
- * Thermal Fault Protection
- * Compact package: DFN3X3-10

ORDERING INFORMATION

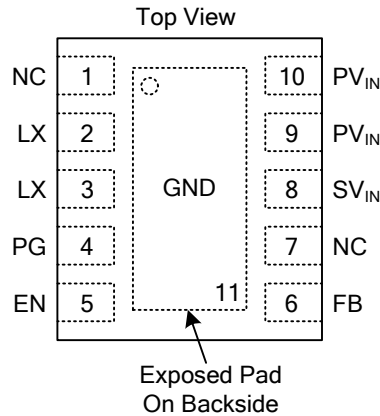
| Ordering Number | Package | Packing |
|---------------------|-------------|-----------|
| UD05301G-K10-3030-R | DFN-10(3x3) | Tape Reel |

| | |
|---|---|
| <p>UD05301G-K10-3030-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p> | <p>(1) R: Tape Reel</p> <p>(2) K10-3030: DFN-10(3x3)</p> <p>(3) G: Halogen Free and Lead Free</p> |
|---|---|

MARKING



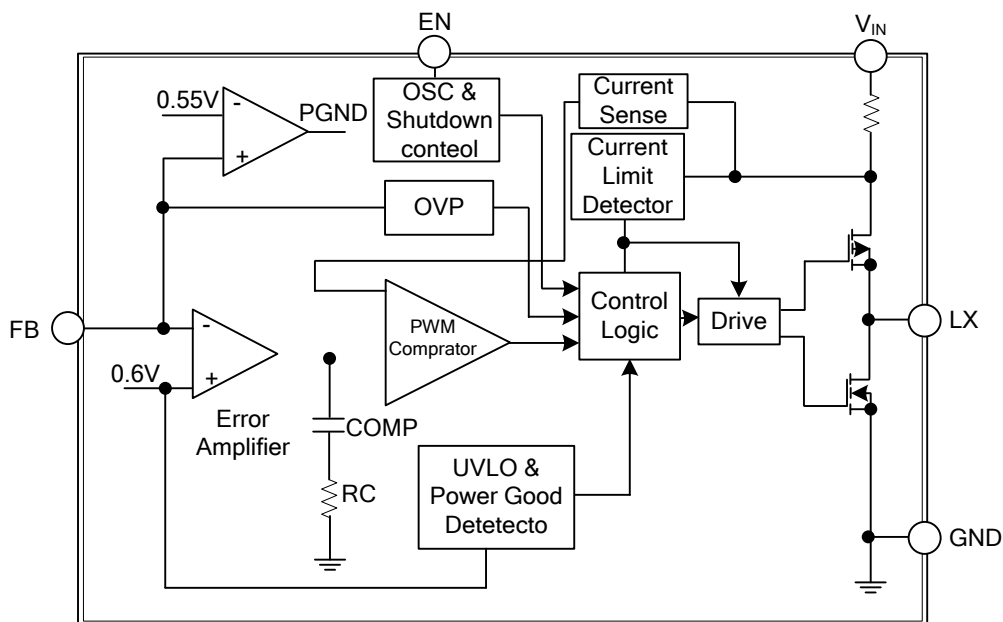
■ PIN CONFIGURATION



■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---------|------------------|---|
| 1, 7 | NC | No connection. |
| 2, 3 | LX | Switch Output. Connect this pin to the switching end of the inductor. |
| 4 | PG | Power Good Indicator. Pull-High Resistor is Needed. |
| 5 | EN | On/Off Control Input. Pull EN above 1.5V to turn the device on. |
| 6 | FB | Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V. |
| 8 | SV _{IN} | Signal Input. Drive 2.7V~5.5V voltage to this pin to power on this chip. Connecting a 1uF(min)ceramic bypass capacitor between SVIN and GND to eliminate noise |
| 9, 10 | PV _{IN} | Power Supply Input. Drive 2.7V~5.5V voltage to this pin to power on this chip. Connecting a 10uF(min)ceramic bypass capacitor between PVIN and GND to eliminate noise |
| 11 | GND | Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. |

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|--|-----------|---------------------|------------------|
| Supply Voltage | V_{IN} | 6 | V |
| | V_{LX} | -0.3~ V_{IN} +0.3 | V |
| All Other Pins | | -0.3~+6 | V |
| Power Dissipation ($T_A=25^\circ\text{C}$) | P_D | 1.43 | W |
| Junction Temperature | T_J | 150 | $^\circ\text{C}$ |
| Storage Temperature | T_{STG} | -65~+150 | $^\circ\text{C}$ |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Stresses exceed those ratings may damage the device.

■ RECOMMENDED OPERATING CONDITIONS

| | | | |
|----------------------|-----------|---------|------------------|
| Input Supply Voltage | V_{IN} | 2.7~5.5 | V |
| Output Voltage | V_{OUT} | 0.6~5.5 | V |
| Ambient Temperature | T_A | -40~+85 | $^\circ\text{C}$ |
| Junction Temperature | T_J | -40~125 | $^\circ\text{C}$ |

Note: If out of its operation conditions, the device is not guaranteed to function.

■ THERMAL RESISTANCES CHARACTERISTICS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-------------------------|---------------|---------|--------------------|
| Junction ambient (Note) | θ_{JA} | 72 | $^\circ\text{C/W}$ |
| Junction to Case | θ_{JC} | 10 | $^\circ\text{C/W}$ |

Note: The PCB area is 4 times larger than that of IC's

■ ELECTRICAL CHARACTERISTICS ($V_{IN}=5\text{V}$, $T_A=25^\circ\text{C}$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------|---|-------|-------|-------|------------------|
| Input Voltage Range | V_{IN} | | 2.7 | | 5.5 | V |
| Quiescent Current | I_Q | $V_{EN}=V_{IN}$, $V_{FB}=0.65\text{V}$ | | 550 | | μA |
| Shutdown Current | I_S | $V_{EN}=0\text{V}$, $V_{IN}=5.5\text{V}$ | | 0.1 | 1 | μA |
| IN Under Voltage Lockout Threshold | UVLO | Rising Edge | | 2.2 | | V |
| IN Under Voltage Lockout Hysteresis | | | | 0.2 | | V |
| Regulated FB Voltage | | | 0.582 | 0.6 | 0.618 | V |
| FB Input Current | I_{FB} | $V_{FB}=0.65\text{V}$ | -50 | | 50 | nA |
| PFET On Resistance (Note) | $R_{(ON)P}$ | $I_{SW}=200\text{mA}$ | | 0.085 | | Ω |
| NFET On Resistance (Note) | $R_{(ON)N}$ | $I_{SW}=-200\text{mA}$ | | 0.065 | | Ω |
| SW Leakage Current | | | -1 | | 1 | μA |
| PFET Current Limit | | Duty Cycle=100%, Current Pulse Width <1ms | 3.2 | 3.5 | | A |
| Oscillator Frequency | F_{SW} | $V_{IN}=3.6\text{V}$, $I_{OUT}=300\text{mA}$ | 1 | 1.2 | 1.4 | MHZ |
| Maximum Duty Cycle | | | | 100 | | % |
| Minimum On-Time (Note) | T_{ON} | | | 80 | | nS |
| Thermal Shutdown Trip Threshold (Note) | | | | 150 | | $^\circ\text{C}$ |
| EN High-Level Input Voltage | | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | 1.5 | | | V |
| EN Low-Level Input Voltage | | | | | 0.4 | V |
| EN Input Current | I_{EN} | $V_{EN}=0\text{V} \sim 5.5\text{V}$ | -1 | | 1 | μA |

Note: Guaranteed by design.

■ TYPICAL APPLICATION CIRCUIT

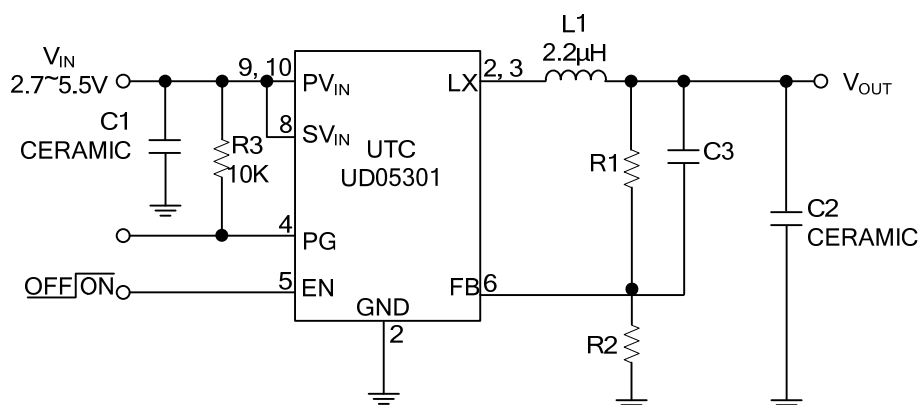


Table 1. Recommended Component Selection

| V _{OUT} | C1 | R1 | R2 | C3 | L1 | C2 |
|------------------|--------|-------|------|--------|-------|--------|
| 3.3V | 22μF×2 | 30.5K | 6.8K | Option | 2.2μH | 22μF |
| 2.5V | 22μF | 15K | 4.7K | Option | 2.2μH | 22μF |
| 1.8V | 22μF | 20K | 10K | Option | 2.2μH | 22μF |
| 1.2V | 10μF | 20K | 20K | Option | 1.2μH | 22μF×2 |
| 1.0V | 10μF | 20K | 30K | Option | 1.2μH | 22μF×2 |

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