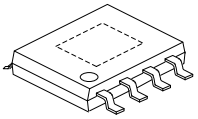
UD40302 **LINEAR INTEGRATED CIRCUIT**

40V, 3A, 220KHZ ASYNCHRONOUS STEP-DOWN CONVERTER



HSOP-8

■ DESCRIPTION

The UTC **UD40302** is a monolithic step-down switch mode converter with a built-in high-side power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The UTC **UD40302** provides a very compact system solution and good thermal conductance.

■ FEATURES

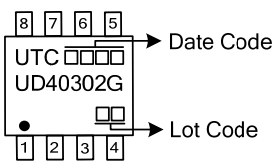
* Wide Input Voltage from 9V to 40V
* Up to 3A Output Current
* High Efficiency Up to 93%
* Internal Soft-Start
* Auto Recovery after Faults
* Output Cord Voltage Drop Compensation
* Programmable Over Current Setting
* Over-Temperature Protection

■ ORDERING INFORMATION

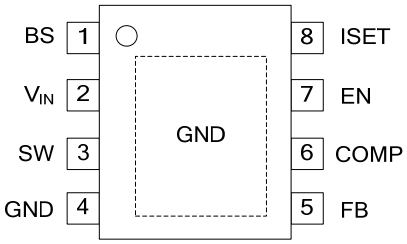
Ordering Number	Package	Packing
UD40302G-SH2-R	HSOP-8	Tape Reel

UD40302G-SH2-R (1)Packing Type (2)Package Type (3)Green Package	 (1) R: Tape Reel (2) SH2: HSOP-8 (3) G: Halogen Free and Lead Free

■ MARKING



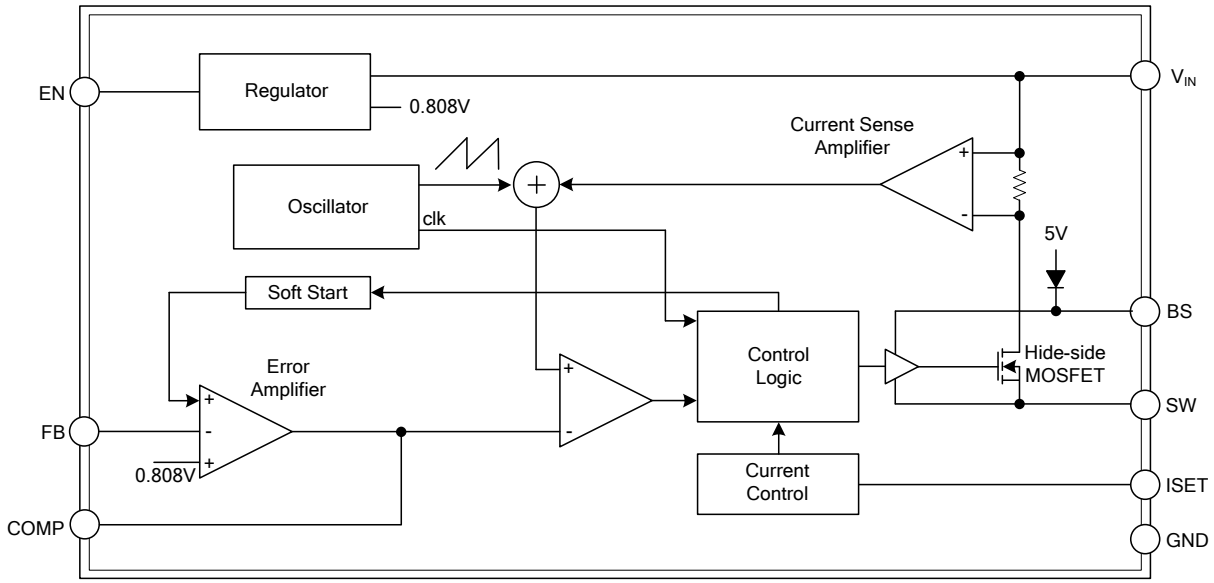
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	BS	High Side Gate Drive Boost Input. A 22nF or greater capacitor must be connected from this pin to SW. It can boost the gate drive to fully turn on the internal high side NMOS.
2	V_{IN}	Power Supply Input Pin. Drive 9V to 40V voltage to this pin to power on this chip. Connecting a bypass capacitor (≧22μFx2) between V_{IN} and GND to eliminate noise.
3	SW	Power Switching Output. It is the output pin that internal high side NMOS switching to supply power.
4	GND	Ground Pin.
5	FB	Voltage Feedback Input Pin. Connecting FB and V_{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulate it at 0.808V.
6	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series R_C network from COMP pin to GND.
7	EN	Enable Input Pin. This pin provides a digital control to turn the converter on or off. The pin could be floated for self-startup.
8	ISET	Output Current Setting Pin. Connect a resistor between ISET and GND pin to set output current.
9	GND	Exposed Pad. Connecting to Pin 4.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Supply Voltage	V_{IN}	-0.3 ~ 42	V
SW Voltage	V_{SW}	-0.3 ~ 42	V
Boost Voltage	V_{BS}	-0.3 ~ (V_{SW}+6)	V
All Other Pins Voltage		-0.3 ~ 6	V
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Stresses exceed those ratings may damage the device.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Input Supply Voltage	V_{IN}	9 ~ 40	V
Ambient Temperature	T_A	-40 ~ +85	°C
Junction Temperature	T_J	-40 ~+125	°C

Note: If out of its operation conditions, the device is not guaranteed to function.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction To Ambient	θ_{JA}	105	°C/W
Junction to Case	θ_{JC}	50	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{IN}=12V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
Quiescent Current (Non-Switching)	I_Q	V_{EN}=3.0V, V_{FB}=1V		0.9	1.4	mA
Standby Supply Current (No Loading)		V_{EN}=3.0V, V_{OUT}=5V		3.0		mA
Shutdown Current		V_{EN}=0V		75	115	μA
Reference Voltage						
Feedback Voltage	V_{FB}	10V≤V_{IN}≤38V	792	808	824	mV
Input UVLO						
UVLO Threshold		V_{IN} Rising	8.0	8.5	8.9	V
Hysteresis		V_{IN} Falling		1.2		
Oscillator						
Switching Frequency	f_{SW}	V_{FB}=0.808V	170	220	270	kHz
Foldback Switching Frequency		V_{FB}=0V		30		kHz
Maximum Duty Cycle	D_{MAX}		85	88	91	%
Minimum On Time	$T_{ON(MIN)}$	V_{FB}=0.7V		200		ns
EN Logic Threshold						
EN High-Level Input Voltage	V_{ENH}		2.0			V
EN Low-Level Input Voltage	V_{ENL}				0.4	V
EN Pull-Up Current				4		μA
MOSFET						
High Side MOSFET On Resistance (Note)	$R_{DS(on)h}$	At 25°C		110		mΩ
High-Side MOSFET Leakage Current		V_{EN}=0V, V_{SW}=0V			10	μA
Current Limit						
Current Limit (Note)	I_{LIM}	L=30μH		4.5		A
Error Amplifier						
Error Amplifier Transconductance (Note)	G_{EA}	ΔI_{COMP}=±10μA		650		μA/V
Error Amplifier Voltage Gain (Note)	A_{EA}			4000		V/V
Current Sense Transconductance (Note)	G_{CS}			5.25		A/V
Current Setting						
ISET Voltage				1		V
ISET to I_{OUT} Current Gain		I_{OUT}/ISET, R_{ISET}=19.6kΩ		25000		A/A
Current Controller DC Accuracy		R_{ISET}=19.6kΩ , V_{OUT}=3.5V, Open-Loop DC Test	1175	1190	1205	mA
Thermal Shutdown						
Thermal Shutdown Threshold (Note)				150		°C

Note: Guaranteed by design.

■ FUNCTION DESCRIPTION

The **UD40302** is a constant frequency current mode step-down asynchronous DC/DC converter. It regulates input voltage from 9V to 40V, down to an output voltage as low as 1V, and can provide up to 3A of continuous load current.

Control Loop

During normal operation, the output voltage is sensed at FB pin through a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output pin – COMP is compared to the switch current to controls the RS latch. At each cycle, the high side NMOS would be turned on when the oscillator sets the RS latch and would be turned off when current comparator resets the RS latch. When the load current increases, the FB pin voltage drops below 0.808V, it causes the COMP voltage increase until average inductor current arrive at new load current.

Input Under Voltage Lockout

When the **UD40302** power on, the internal circuits are held inactive until V_{IN} exceeds the input UVLO threshold voltage. And the regulator will be disabled when V_{IN} below the input UVLO threshold voltage.

Over Current Protection

ISET pin is connected to a resistor to set output current limit value. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The oscillator normally switches at 220kHz. However, if the FB voltage drops down, then the switching frequency decreases. Oncethe overload condition is removed, the frequency will return to normal.

Over Temperature Protection

The **UD40302** incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown.

Compensation

The stability of the feedback circuit is controlled through COMP pin. The compensation value of the application circuit is optimized for particular requirements. If different conversions are requires, some of the components may need to be changes to ensure stability.

■ APPLICATION INFORMATION

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.808V. Thus the output voltage is:

$$V_{OUT} = 0.808\times(1+\frac{R1}{R2})\ V$$

Table1 lists recommended values of R1 and R2 for most used output voltage:

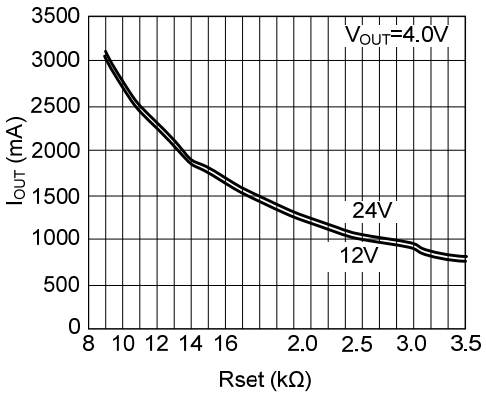
V_{OUT}	R1	R2
5V	52kΩ	10kΩ
3.3V	30.9kΩ	10kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Current Limit Setting

UD40302 current limit value is set by a resistor connected between the ISET pin and GND. The output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 25000 (25mA/1μA).

To determine the proper resistor for a desired current, please refer to below:



Current Limit Line Compensation

When operating at current limit mode, the current limit increase slightly with input voltage. For wide input voltage application, a resistor R_C is added to compensate line change and keep output high current limit accuracy, as shown in Figure1.

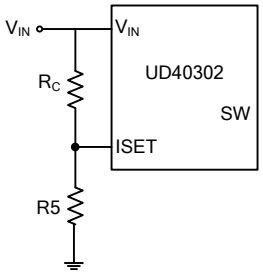


Figure 1. Input Line Compensation

■ APPLICATION INFORMATION (Cont.)

Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IIN(RMS)} = I_{OUT} \times \sqrt{D \times (1 \times D)}$$

Where D is the duty cycle and the value is V_{OUT} / V_{IN}. A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred. Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100uF or 470uF low ESR electrolytic capacitor when operated in high input voltage range (V_{IN} > 20V). It can improve the device's stability. The output ripple voltage ΔV_{OUT} is described as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_2}\right)$$

Where f_S is the switching frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, RESR is the equivalent series resistance value of the output capacitor, and the C2 is the output capacitor. When using the ceramic capacitors, the RESR can be ignored and the output ripple voltage ΔV_{OUT} is shown as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \cdot f_S^2 \cdot L \cdot C_2} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage ΔV_{OUT} can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The **UD40302** can be optimized for a wide range of capacitance and ESR values.

Inductor

The output inductor is used for store energy and filter output ripple current. A large value inductor will result in less ripple current and lower output ripple voltage. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and results in lower output ripple voltage. A good rule for determining the inductance is set the peak-to-peak inductor ripple current ΔI almost equal to 30% of the maximum load current. Then the minimum inductance can be calculated with the following equation:

$$L \geq \frac{V_{OUT}}{f_S \cdot \Delta I} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$\Delta I = 0.3 \times I_{ILOAD(MAX)}$$

■ APPLICATION INFORMATION (Cont.)

Where V_{IN} is the input voltage, fS is the switching frequency, ΔI is the peak-to-peak inductor ripple current and $I_{LOAD(MAX)}$ is the maximum load current.

Choose an inductor that will cause the peak inductor current satisfying the equation:

$$I_{LP} = I_{LOAD(MAX)} + \frac{V_{OUT}}{2 \cdot f_S \cdot L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \leq I_{LIMIT}$$

Where I_{LIMIT} is the high-side MOSFET current limit value.

Rectifier Diode

During the transition between switching MOSFETs, a Schottky diode should be connected between SW pin and GND pin. The Schottky diode must have current rating higher than the maximum.

Compensation Components

The system stability and transient response are controlled through the COMP pin. Selecting the appropriate compensation value by the following procedure:

1. Calculate the R3 value with the following equation:

$$R_3 < \frac{2\pi \cdot C_2 \cdot f_S \cdot V_{OUT}}{10 \cdot G_{EA} \cdot G_{CS} \cdot V_{FB}}$$

where GEA is the error amplifier transconductance, and GCS is the current sense transconductance.

2. Calculate the C3 value with the following equation:

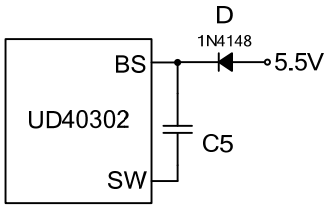
$$C_3 > \frac{4 \cdot 10}{2\pi \cdot R_3 \cdot f_S}$$

3. If the C2 ESR zero is less than half of the switching frequency, use C6 to cancel the ESR zero:

$$C_6 > \frac{C_2 \cdot R_{ESR}}{R_3}$$

External Boost Diode Selection

For duty cycle larger than 65% applications, it is recommended that an external boost diode be added. This helps improve the efficiency. The boost diode can be a low cost one such as 1N4148.



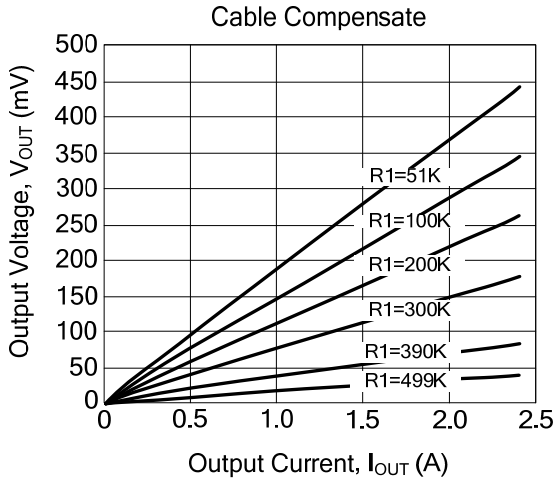
■ PCB LAYOUT RECOMMENDATION:

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show bellow:

1. Keep the traces of the main current paths as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} bypass capacitor (CIN) close to the device pins (V_{IN} and GND). The loop area formed by CIN and V_{IN}/GND pins must be minimized.
3. Place feedback resistors close to the FB pin. Connect feedback network behind the output capacitors.
4. Place compensation components close to the COMP pin.
5. Keep the sensitive signal (FB, COMP, ISET) away from the switching signal (SW).
6. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacities.
7. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.
8. Multi-layer PCB design is recommended.

■ STABILITY COMPENSATION

R1 is the high side resistor of voltage divider. In the case of high R1 used, the frequency compensation needs to be adjusted correspondingly. As show in Typical application circuit, adding a capacitor(C7) in paralled with R1 or increasing the compensation capacitance(C3、C6) at COMP pin helps the system stability.



■ TYPICAL APPLICATION CIRCUIT

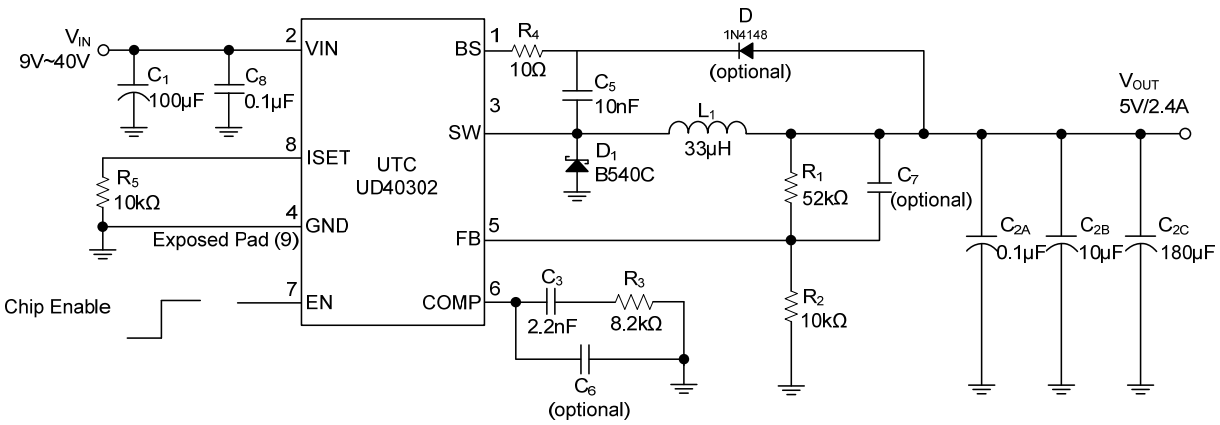


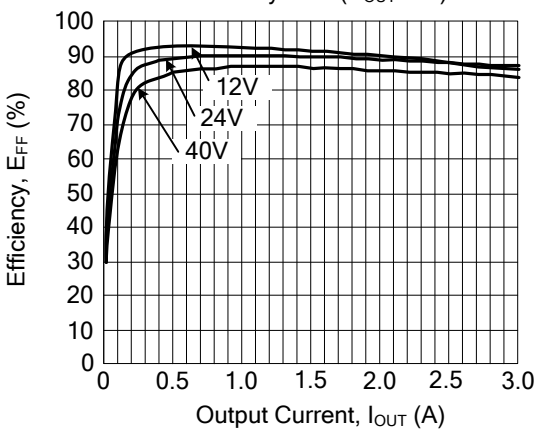
Table 1 Recommended Component Selection

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	C_3 (nF)	C_6	L_1 (µH)	C_{2A} (µF)	C_{2B} (µF)
5	52	10	8.2	2.2	NA	47	10 6.3V/Ceramic	180 6.3V/30mΩ
5	52	10	8.2	2.2	NA	47	10 6.3V/Ceramic	470 6.3V/30mΩ

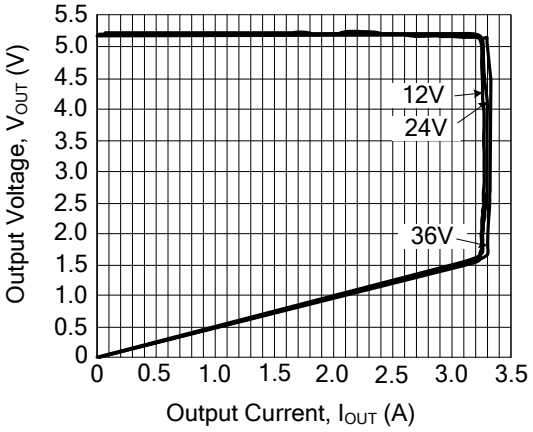
■ TYPICAL CHARACTERISTICS

C1=100μF, C2=330μF, L1=33μH, T_A=25°C

Efficiency Test (V_{OUT}=5V)

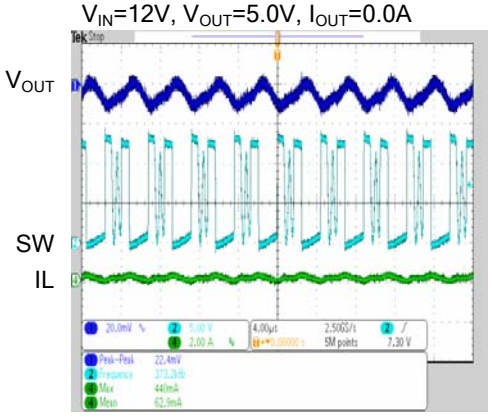


CC/CV Curve



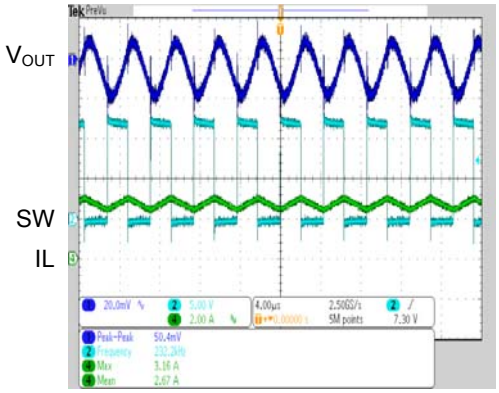
Steady State

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=0.0A



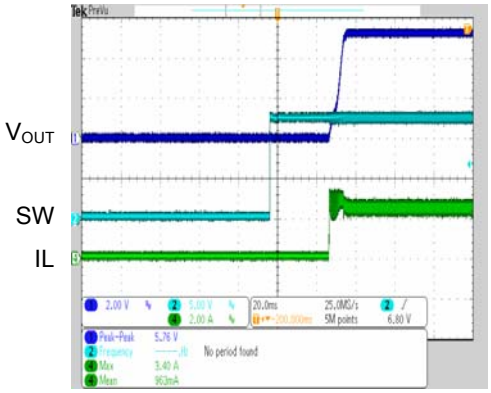
Steady State

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=3A



Power On

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=2.4A



Shut Down

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=2.4A