

UTC UNISONIC TECHNOLOGIES CO., LTD

LR2965 **Preliminary CMOS IC**

1.5A, LOW DROPOUT REGULATOR WITH POWER **GOOD**

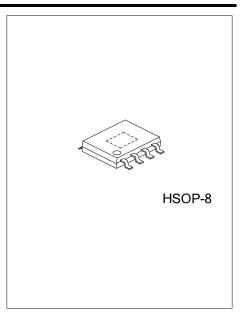
DESCRIPTION

The UTC LR2965 is CMOS-based positive voltage and a very low dropout regulator IC that minimum input voltage is 2.5V and is capable of delivering the continuous output load current up to 1.5A.

It has features of low dropout (maximum 300mV at 1A), a very low quiescent current (typically 300uA at 0.1A) and very high PSRR up to 86dB at 1A load current.

The output voltage can be set from 0.5V to $(V_{\text{IN}}$ - $V_{\text{D}})$ with an external resistor divider and it has ±2% accuracy through all temperature ranges include the line as well as load variations. It is allowed to use a small 4.7µF MLCC input and output capacitor to deliver the current with the stable operation.

Built-in Soft-Start function reduces the inrush current and the other features are include over current protection (OCP), short-circuit protection (SCP), and thermal shut down protection (TSD).



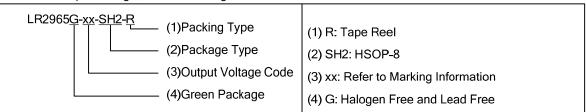
FEATURES

- * Input Voltage Range: 2.5V~6.0V * Supply Current: (Typ.) 300uA
- * Current limit: (Min.) 1.8A
- * Adjustable Output from 0.5V
- * LR2965: Typ 0.4V Dropout @ I_{OUT}=1.5A
- * Compatible with MLCC Capacitors
- * Built-in Soft-Start Limits Inrush Current
- * Built-in Thermal Shutdown Protection
- * Built-in Over Current & Short Circuit Protection

ORDERING INFORMATION

Ordering Number	Package	Packing
LR2965G-xx-SH2-R	HSOP-8	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

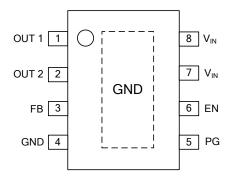


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■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING		
HSOP-8	25: 2.5V AD: ADJ	8 7 6 5 ☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐		

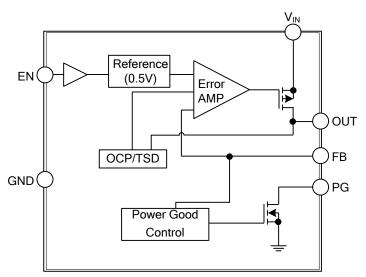
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1, 2	OUT	Voltage Regulator Output Pin
3	FB	Feedback Pin. Connect to output through a voltage-divider to set the output. Recommended that the tolerance of feedback resistors is below 1%.
4	GND	Ground Pin
5	PG	Open Drain Power-Good (PG) Output.
6	EN	Chip Enable Pin
7,8	V _{IN}	Input Supply Voltage Pin.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	-0.3~7	V
Output Voltage	OUT	-0.3~V _{IN} +0.3	V
Junction Temperature	TJ	150	°C
Storage Temperature	T _{STG}	-65~150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	2.5~6.0	V
Ambient Temperature Range	T _A	-40~85	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	50	°C/W
Junction to Case	θ _{JC}	10	°C/W

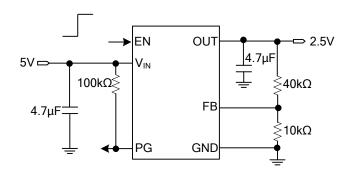
■ ELECTRICAL CHARACTERISTICS

All parameters are guaranteed over the operational supply voltage and temperature range. Operating conditions unless otherwise noted are: V_{IN} =5V, OUT=2.5V and T_A =25°C. Typical values are for information only.

Supply Voltage Curescent Current Io IouT=100mA 300 UA						NANY	LINIT
Company Comp	PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown Current I_STD VIN=6V, VEN=GND 0.2 2 UA			I		T		
Feedback (FB)						_	
Feedback Voltage Accuracy	Shutdown Current	I _{STD}	V_{IN} =6V, V_{EN} =GND		0.2	2	uA
Part	Feedback (FB)	1		1	1	1	
Dutput (OUT) Output Accuracy Vout -2 2 % Load Regulation R _{LO} I _{OUT} =1mA to 1.5A 0.1 2 %/A Line Regulation R _{LN} V _{IN} =2.2~6V, V _{OUT} =1.225V, I _{OUT} =1mA -0.2 0.2 %/V Dropout Voltage V _D I _{OUT} =1.5A, V _{FB} =480mV 400 400 400 600	Feedback Voltage Accuracy	V_{F}	I _{OUT} =10mA, T _A =25°C	490	500	510	mV
Dutput Accuracy	Input Bias Current	I _F	V_{FB} =0.5V, V_{IN} =6V		0.001	0.1	uA
Load Regulation R _{LO} I _{OUT} =1mA to 1.5A 0.1 2 %/A Line Regulation R _{LN} V _{IN} =2.2~6V, V _{OUT} =1.225V, I _{OUT} =1mA -0.2 0.2 %/V Dropout Voltage V _D I _{OUT} =1.5A,V _{FB} =480mV 400 W Current Limit I _C 1.8 A Load transient (Note 1) L _{OT} I _{OUT} =20mA to 1.5A, 3 % Line Transient (Note 1) R _{NT} ΔV _{IN} =0.5V 3 % Enable (EN)) V _{ENL} EN rising, V _{IN} =0UT+1V~6V 1.2 6 V Input Threshold V _{ENL} EN falling, V _{IN} =0UT+1V~6V 1.2 6 V Input Bias Current I _{EN} EN=0 or 6V -1 0 1 uA Power Good (PG) P _{V1} FB high, V _{HYS} =10mV, V _{IN} =0UT+1V~6V 550 mV Pvus FB low, V _{HYS} =10mV, V _{IN} =0UT+1V~6V 400 mV Dutput Voltage Low P _{CL} FB=0.4V or 0.6V, I _{PG} =1mA 25 200 mV Dutput Current High P _{CH}	Output (OUT)						
Composition Right Vin=2.2~6V, Vout=1.225V, Iout=1mA -0.2 0.2 %/V	Output Accuracy	V_{OUT}		-2		2	%
Corporative V_D	Load Regulation	R_{LO}	I _{OUT} =1mA to 1.5A		0.1	2	%/A
Corporat Voltage V _D I _{OUT} =1A,V _{FB} =480mV 140 280 mV Current Limit I _C 1.8 A Load transient (Note 1) LoT I _{OUT} =20mA to 1.5A, 3 % Line Transient (Note 1) R _{NT} ΔV _{IN} =0.5V 3 % Enable (EN)) Input Threshold V _{ENL} EN rising, V _{IN} =OUT+1V~6V 1.2 6 V Input Bias Current I _{EN} EN=0 or 6V -1 0 1 uA Power Good (PG) Threshold Voltage P _{V1} FB high, V _{HYS} =10mV, V _{IN} =OUT+1V~6V 550 mV Putput Voltage Low P _{CL} FB=0.4V or 0.6V, I _{PG} =1mA 25 200 mV Output Voltage Low P _{CL} FB=0.4V or 0.6V, I _{PG} =1mA 25 200 mV Output Current High P _{CH} P _{WRGD} =6V 0.001 0.1 uA Rising Delay Time P _{RDT} From FB*90% to PG 10 us Falling Delay Time 2 P _{FDT2} V _{IN} =6V, From	Line Regulation	R_{LN}	V _{IN} =2.2~6V, V _{OUT} =1.225V, I _{OUT} =1mA	-0.2		0.2	%/V
IouT=0.5A,VFB=480mV			I _{OUT} =1.5A,V _{FB} =480mV		400		mV
Current Limit	Dropout Voltage	V_D	I _{OUT} =1A,V _{FB} =480mV		140	280	
Load transient (Note 1)			I _{OUT} =0.5A,V _{FB} =480mV			200	
The shold Current High Pour P	Current Limit	I _C		1.8			Α
Name	Load transient (Note 1)	L _{OT}	I _{OUT} =20mA to 1.5A,		3		%
Name	Line Transient (Note 1)	R _{NT}	$\Delta V_{IN}=0.5V$		3		%
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Enable (EN))						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Local Theoretical I	V_{ENH}	EN rising, V _{IN} =OUT+1V~6V	1.2		6	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input inresnoid	V _{ENL}	EN falling, V _{IN} =OUT+1V~6V			0.4	
Threshold Voltage $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Bias Current			-1	0	1	uA
Threshold Voltage P_{V2} FB low, V_{HYS} =10mV, V_{IN} =OUT+1V~6V $\frac{1}{400}$ mV Output Voltage Low P_{CL} FB=0.4V or 0.6V, I_{PG} =1mA $\frac{1}{25}$ 200 mV Output Current High $\frac{1}{25}$ PwRgD=6V $\frac{1}{25}$ 0.001 0.1 uA Rising Delay Time $\frac{1}{25}$ From FB*90% to PG $\frac{1}{25}$ 10 us Falling Delay Time 1 $\frac{1}{25}$ V _{IN} =2.5V, From FB to PG $\frac{1}{25}$ 0.001 us Thermal Shutdown (TSD) (Note 1)	Power Good (PG)						
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Thursday 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	P _{V1}	FB high, V _{HYS} =10mV, V _{IN} =OUT+1V~6V		550		mV
Output Voltage Low P _{CL} FB=0.4V or 0.6V, I _{PG} =1mA 25 200 mV Output Current High P _{CH} P _{WRGD} =6V 0.001 0.1 uA Rising Delay Time P _{RDT} From FB*90% to PG 10 us Falling Delay Time 1 P _{FDT1} V _{IN} =2.5V, From FB to PG 20 70 120 us Falling Delay Time 2 P _{FDT2} V _{IN} =6V, From FB to PG 60 180 300 us Thermal Shutdown (TSD) (Note 1) TSD On 165 165 165	Threshold Voltage	P _{V2}	FB low, V _{HYS} =10mV, V _{IN} =OUT+1V~6V		400		mV
Rising Delay Time P_{RDT} From FB*90% to PG 10 us Falling Delay Time 1 P_{FDT1} V_{IN} =2.5V, From FB to PG 20 70 120 us Falling Delay Time 2 P_{FDT2} V_{IN} =6V, From FB to PG 60 180 300 us Thermal Shutdown (TSD) (Note 1) T_{SDON} TSD On 165	Output Voltage Low		FB=0.4V or 0.6V, I _{PG} =1mA		25	200	mV
Falling Delay Time 1 P _{FDT1} V _{IN} =2.5V, From FB to PG 20 70 120 us Falling Delay Time 2 P _{FDT2} V _{IN} =6V, From FB to PG 60 180 300 us Thermal Shutdown (TSD) (Note 1) TSD On 165 165	Output Current High	P _{CH}	P _{WRGD} =6V		0.001	0.1	uA
Falling Delay Time 1 P _{FDT1} V _{IN} =2.5V, From FB to PG 20 70 120 us Falling Delay Time 2 P _{FDT2} V _{IN} =6V, From FB to PG 60 180 300 us Thermal Shutdown (TSD) (Note 1) TSD Threshold 165 165	Rising Delay Time	P _{RDT}	From FB*90% to PG		10		us
Thermal Shutdown (TSD) (Note 1) TSD Threshold TSDON TSD On 165	Falling Delay Time 1		V _{IN} =2.5V, From FB to PG	20	70	120	us
Thermal Shutdown (TSD) (Note 1)	Falling Delay Time 2	P _{FDT2}	V _{IN} =6V, From FB to PG	60	180	300	us
ISD Threshold	Thermal Shutdown (TSD) (Note 1)						
ISD Infestion	TSD Threshold	T _{SDON}	TSD On		165		
		T _{SDOFF}	TSD Off		145		_

Note: Guaranteed by design but not production tested.

TYPICAL APPLICATION CIRCUIT



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