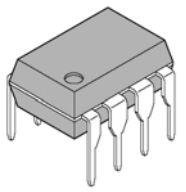
http://www.junyi-ic.com TEL:0755-29955070 FAX:0755-27858707

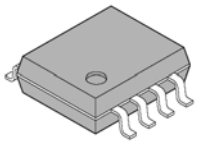
Real-time Clock/Calendar BL5363

DESCRIPTION

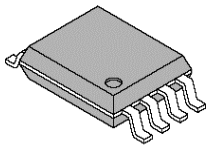
The BL5363 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage-low detector are also provided. All address and data are transferred serially via a two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbits/s. The built-in word address register is incremented automatically after each written or read data byte.



DIP8



SOP8



TSSOP8

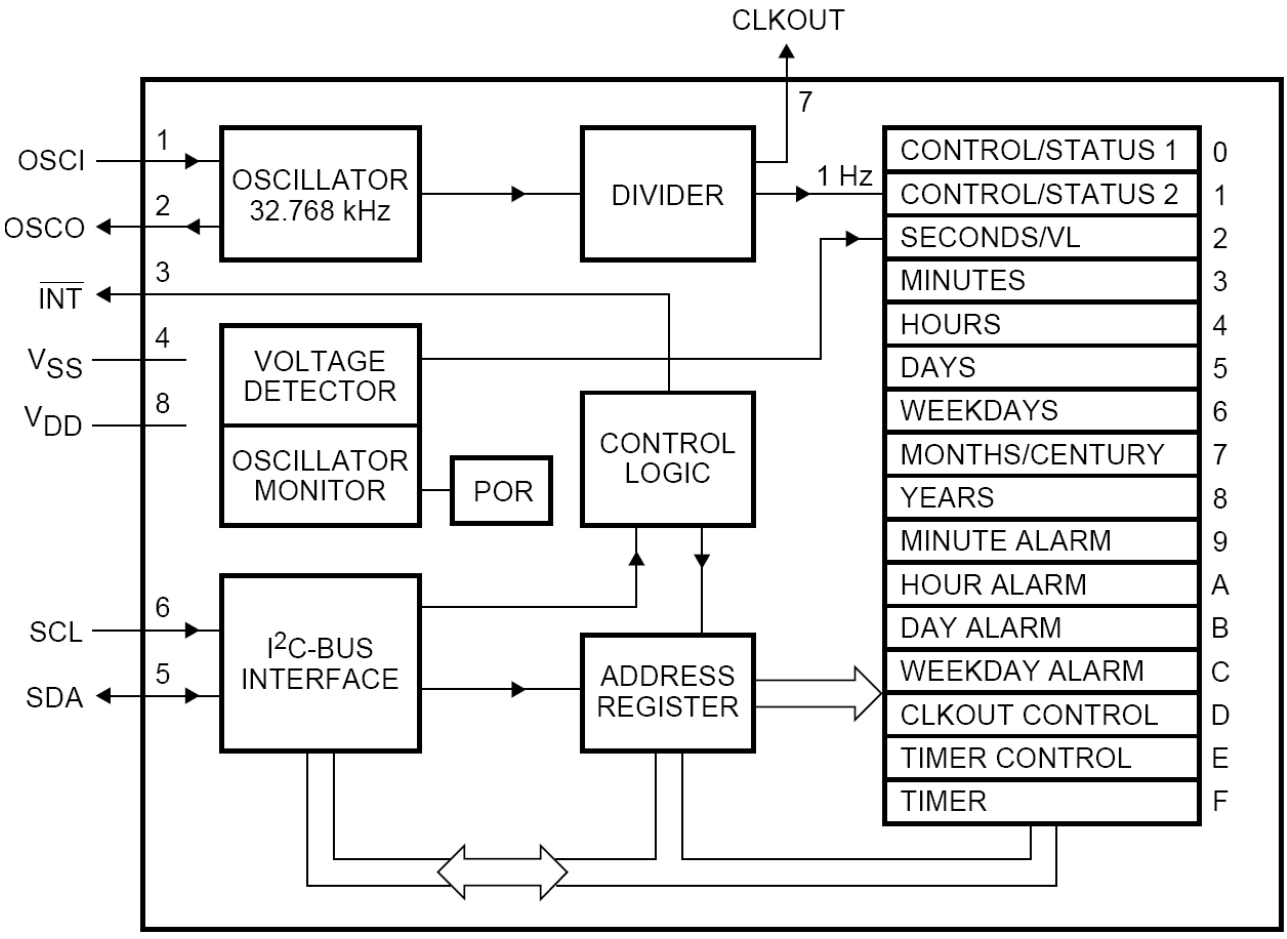
FEATURES

- Provides year, month, day, weekday, hours, minutes and seconds based on32.768 kHz quartz crystal
- Century flag
- Wide operating supply voltage range: 1.0 to 5.0 V
- Low back-up current; typical 0.25 µA at V_{DD} = 3.0 V and Tamb = 25 °C
- 400 kHz two-wire I^2C-bus interface (at V_{DD} = 1.8 to 5.0 V)
- Programmable clock output for peripheral devices: 32.768 kHz, 1024 Hz, 32 Hz and 1 Hz
- Alarm and timer functions
- Voltage-low detector
- Integrated oscillator capacitor
- Internal power-on reset
- I^2C-bus slave address: read A3H; write A2H
- Open drain interrupt pin.

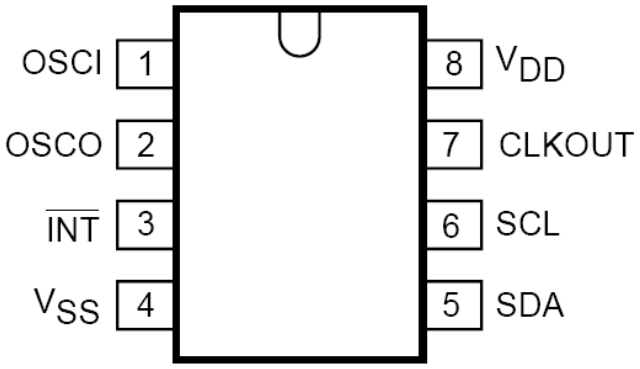
APPLICATIONS

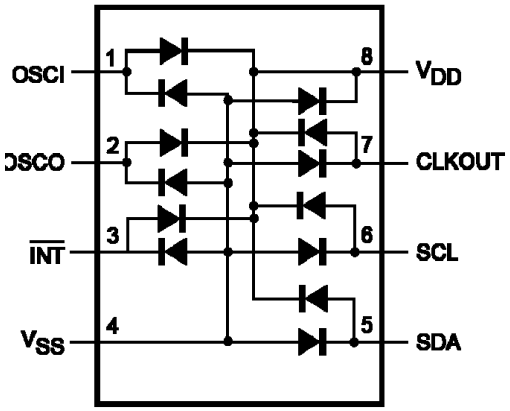
- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products

BLOCK DIAGRAM



PIN CONFIGURATION





Symbol	Pin	Description
OSC1	1	Oscillator input
OSCO	2	Oscillator output
INT	3	Interrupt output(open-drain; active LOW)
Vss	4	Ground
SDA	5	Serial data I/O
CLK	6	Serial clock input
CLKOUT	7	Clock output (open-drain)
V_{DD}	8	Positive supply

ABSOLUTE MAXIMUM RATING（Tamb=25℃）

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.5	+5.5	V
Input Voltage on Inputs SCL and SDA	V_I	-0.5	+5.5	V
Input Voltage on Input OSCI		-0.5	V_{DD}+0.5	V
Output Voltage on Outputs CLKOUT and $\overline{INT}$	Vo	-0.5	+5.5	V
DC Input Current at Any Input	I_I	-10	+10	mA
DC Output Current at Any Output	Io	-10	+10	mA
Total Power Dissipation	Ptot		300	mW
Operating Temperature Range	Topr	-40	+85	℃
Storage Temperature Range	Tstg	-65	+150	℃

STATIC ELECTRICAL CHARACTERISTICS

（Unless otherwise specified， V_{DD} = 1.8 to 5.0 V; Vss = 0 V; Tamb =- 40 to 85° C; f_{OSC} = 32.768 kHz; quartz Rs = 40 kΩ; C_L = 8 pF; ）

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Supplies						
Supply voltage	V_{DD}	I^2C-bus inactive Ta=25° C	1.0*1		5.0	V
		I^2C-bus active f_{SCL}=400kHz	1.8*1		5.0	V
Supply voltage fo Reliable clock/calendar information		Ta=25° C	V_{LOW}		5.0	V
Supply current CLKOUT disabled (FE=0)	I_{DD1}	f_{SCL}=400kHz *2			800	μA
		f_{SCL}=400kHz			200	μA
		f_{SCL}=0Hz; Ta=25° C *2				
		V_{DD}=5V		275	550	nA
		V_{DD}=3V		250	500	nA
		V_{DD}=2V		225	450	nA
		f_{SCL}=0Hz *2				
		V_{DD}=5V		500	750	nA
		V_{DD}=3V		400	650	nA
		V_{DD}=2V		400	600	nA
Supply current CLKOUT enabled (f_{CLKOUT}=32kHz;FE=1)	I_{DD2}	f_{SCL}=0Hz; Ta=25° C *2				
		V_{DD}=5V		825	1600	nA
		V_{DD}=3V		550	1000	nA
		V_{DD}=2V		425	800	nA
		f_{SCL}=0Hz *2				
		V_{DD}=5V		950	1700	nA
		V_{DD}=3V		650	1100	nA
		V_{DD}=2V		500	900	nA
Inputs						
Low-level input voltage	V_{IL}		V_{SS}		$0.3V_{DD}$	V
High-level input voltage	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input leakage current	I_{LI}	V_I=V_{DD} or V_{SS}	-1		+1	μA
Input capacitance	Ci	*3			7	pF
Outputs						
Low-level output current;pin SDA	$I_{OL(SDA)}$	V_{OL}=0.4V; V_{DD}=5V	-3			mA

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Low-level output current;pin $\overline{INT}$	$I_{OL(\overline{INT})}$		-1			mA
Low-level output current;pin CLKOUT	$I_{OL(CLKOUT)}$		-1			mA
High-level output current;pin CLKOUT	$I_{OH(CLKOUT)}$	V_{OH}=4.6V; V_{DD}=5V	1			mA
Output leakage current	I_{LO}	V_O=V_{DD} or V_{SS}	-1		+1	μA
Voltage Detector						
Voltage-low detection level	V_{LOW}	Ta=25° C		0.9	1.0	V

*1 For reliable oscillator start-up at power-up: V_{DD}(min)power-up = V_{DD}(min) + 0.3 V.

*2 Timer source clock = 1¤60 Hz; SCL and SDA = V_{DD}.

*3 Tested on sample basis.

DYNAMIC ELECTRICAL CHARACTERISTICS

（Unless otherwise specified， V_{DD} = 1.8 to 5.0 V; Vss = 0 V; Tamb =- 40 to 85° C; f_{OSC} = 32.768 kHz; quartz Rs = 40 kΩ; C_L = 8 pF; ）

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Oscillator						
Integrated load capacitance	$C_{L(integrated)}$		15	25	35	pF
Oscillator stability	$\Delta f_{OSC}/f_{OSC}$	ΔV_{DD}=200mV Ta=25° C		2×10^{-7}		
Quartz crystal parameters (f_{OSC}=32.768kHz)						
Series resistance	R_S				40	kΩ
Parallel load capacitance	C_L			10		pF
Trimmer capacitance	C_T		5		25	pF
CLKOUT output						
CLKOUT duty factor	δ_{CLKOUT}	*1		50		%
I^2C-bus timing characteristics *2						
SCL clock frequency	f_{SCL}	*3			400	kHz
START condition hold time	$t_{HD;STA}$		0.6			μs
Set-up time for a repeated START condition	$t_{SU;STA}$		0.6			μs
SCL low time	t_{LOW}		1.3			μs
SCL high time	t_{HIGH}		0.6			μs

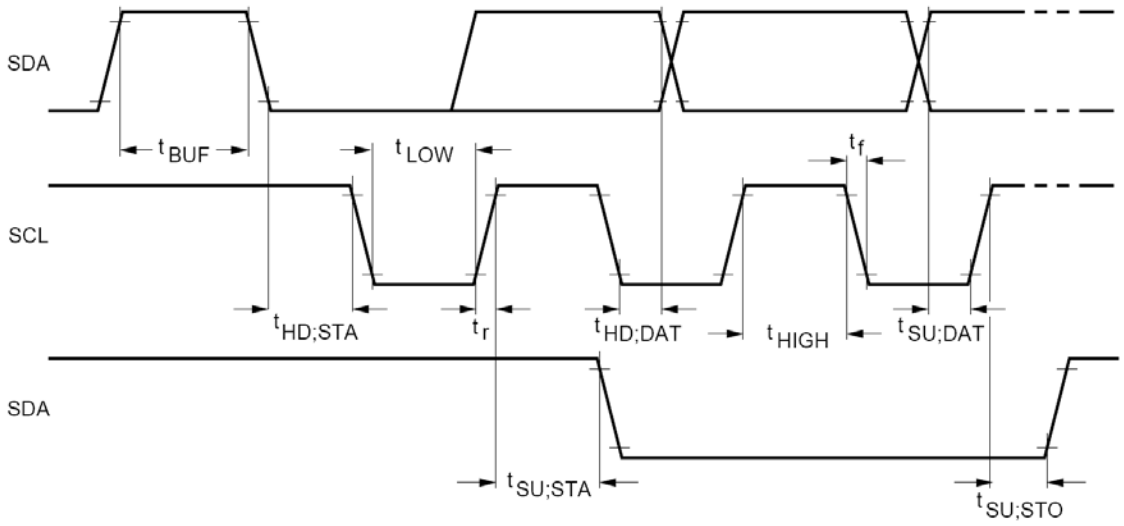
Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
SCL and SDA rise time	tr				0.3	µs
SCL and SDA fall time	tf				0.3	µs
Capacitive bus line load	Cb				400	pF
Data set-up time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns
Set-up time for STOP condition	$t_{SU;STO}$		4.0			µs
Tolerable spike width on bus	t_{SW}				50	µs

*1 Unspecified for f_{CLKOUT} = 32.768 kHz.

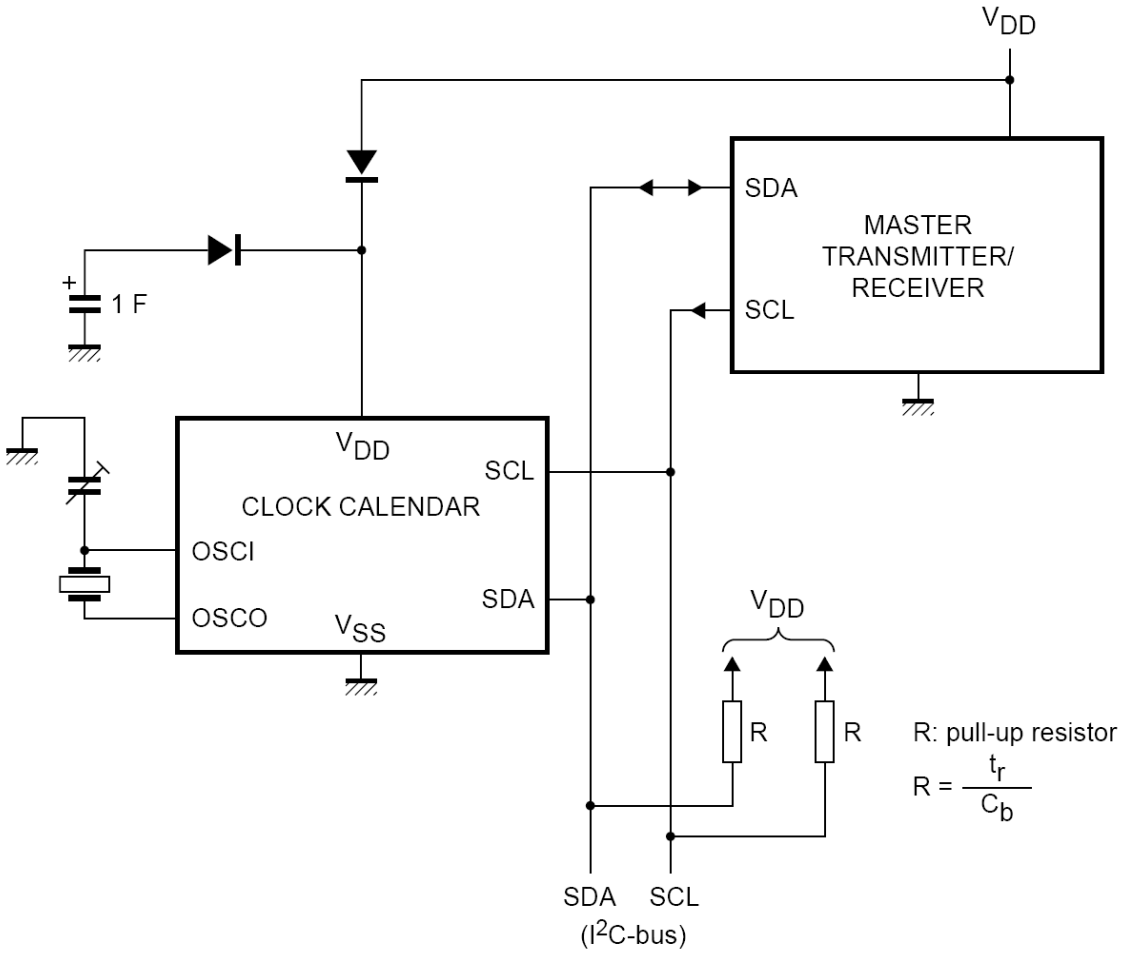
*2 All timing values are valid within the operating supply voltage range at Tamb and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

*3 I^2C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

I2C-bus timing waveforms



APPLICATION CIRCUIT



Method 1: Fixed OSCI capacitor — By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at the CLKOUT pin. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$).

Average deviations of ±5 minutes per year can be easily achieved.

Method 2: OSCI trimmer — The oscillator is tuned to the required accuracy by adjusting a trimmer capacitor on pin OSCI and measuring the 32.768 kHz signal available after power-on at the CLKOUT pin.

Method 3: OSCO output — Direct output measurement on pin OSCO (accounting for test probe capacitance).

APPLICATION SUMMARY

The BL5363 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with an integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00H and 01H) are used as control and/or status registers. The memory addresses 02H through 08H are used as counters for the clock function (seconds up to year counters). Address locations 09H through 0CH contain alarm registers which define the conditions for an alarm. Address 0DH controls the CLKOUT output frequency. 0EH and 0FH are the timer control and timer registers, respectively.

The Seconds, Minutes, Hours, Days, Months, Years as well as the Minute alarm, Hour alarm and Day alarm registers are all coded in BCD format. The Weekdays and Weekday alarm register are not coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

Alarm function modes

By clearing the MSB (bit AE = Alarm Enable) of one or more of the alarm registers, the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag, AF (bit 3 of Control/Status 2 register). The asserted AF can be used to generate an interrupt ($\overline{INT}$). Bit AF can only be cleared by software.

Timer

The 8-bit countdown timer (address 0FH) is controlled by the Timer Control register (address 0EH). The Timer Control register selects one of 4 source clock frequencies for the timer (4096, 64, 1, or 1/60 Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The timer flag TF can only be cleared by software. The asserted timer flag TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. TI/TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

CLKOUT output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the CLKOUT frequency register (address 0DH). Frequencies of32.768 kHz (default), 1024, 32 and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

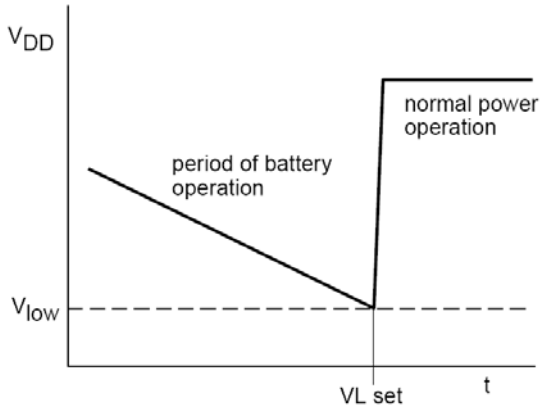
Reset

The BL5363 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE which are set to logic 1.

Voltage-low detector and clock monitor

The BL5363 has an on-chip voltage-low detector. When V_{DD} drops below V_{low} the VL bit (Voltage Low, bit 7 in the Seconds register) is set to indicate that reliable clock/calendar information is no longer guaranteed. The VL flag can only be cleared by software.

Voltage-low detection



The VL bit is intended to detect the situation when V_{DD} is decreasing slowly for example under battery operation. Should V_{DD} reach V_{low} before power is re-asserted then the VL bit will be set. This will indicate that the time may be corrupted.

Registers Organization

Table 1 registers overview

Bit positions labelled as '- 'are not implemented; those labelled with '0' should always be written with logic 0.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	Control/Status 1	TEST1	0	STOP	0	TESTC	0	0	0
01H	Control/Status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
0DH	CLKOUT frequency	FE	–	–	–	–	–	FD1	FD0
0EH	Timer control	TE	–	–	–	–	–	TD1	TD0
0FH	Timer countdown value	<timer countdown value>							

Table 2 BCD formatted registers overview

Bit positions labelled as '- 'are not implemented

Address	Register name	BCD format tens nibble				BCD format units nibble			
		Bit 7 2^3	Bit 6 2^2	Bit 5 2^1	Bit 4 2^0	Bit 3 2^3	Bit 2 2^2	Bit 1 2^1	Bit 0 2^0
02H	Seconds	VL	<seconds 00 to 59 coded in BCD>						
03H	Minutes	–	<minutes 00 to 59 coded in BCD>						
04H	Hours	–	–	<hours 00 to 23 coded in BCD>					
05H	Days	–	–	<days 01 to 31 coded in BCD>					
06H	Weekdays	–	–	–	–	–	<weekdays 0 to 6 > *1		
07H	Months/Century	C	–	–	<months 01 to 12 coded in BCD>				
08H	Years	<years 00 to 99 coded in BCD>							
09H	Minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
0AH	Hour alarm	AE	–	<hour alarm 00 to 23 coded in BCD>					
0BH	Day alarm	AE	–	<day alarm 01 to 31 coded in BCD>					
0CH	Weekday alarm	AE	–	–	–	–	<weekday alarm 0 to 6 > *1		

*1 Not coded in BCD

Control/Status 1 register

Table 3 Control/Status 1 register bits description(address 00H)

Bit	Symbol	Description
7	TEST1	TEST1 = 0; normal mode. TEST1 = 1; EXT_CLK test mode;
5	STOP	STOP = 0; RTC source clock runs. STOP = 1; all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available).
3	TESTC	TESTC = 0; power-on reset override facility is disabled (set to logic 0 for normal operation). TESTC = 1; power-on reset override is enabled.
6, 4, 2 to 0	0	By default set to logic 0.

Control/Status 2 register

Table 4 Description of Control/Status 2 register bits description(address 01H)

Bit	Symbol	Description
7 to 5	0	By default set to logic 0.
4	TI/TP	TI/TP = 0: INT is active when TF is active (subject to the status of TIE).
		TI/TP = 1: INT pulses active according to Table 5 (subject to the status of TIE). Note that if AF and AIE are active then INT will be permanently active.
3	AF	When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. See Table 6 for the value descriptions of bits AF and TF.
2	TF	
1	AIE	Bits AIE and TIE activate or deactivate the generation of an interrupt when AF or TF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set. AIE = 0: alarm interrupt disabled; AIE = 1: alarm interrupt enabled. TIE = 0: timer interrupt disabled; TIE = 1: timer interrupt enabled.
0	TIE	

Table 5 $\overline{\text{INT}}$ operation(bit TI/TP=1)

Source clock (Hz)	$\overline{\text{INT}}$ *1 period (s)	
	n *2 = 1	n > 1
4 096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

*1 TF and INT become active simultaneously.

*2 n = loaded countdown timer value. Timer stopped when n = 0.

Table 6 Value descriptions for bits AF and TF

R/W	Bit: AF		Bit: TF	
	Value	Description	Value	Description
Read	0	alarm flag inactive	0	timer flag inactive
	1	alarm flag active	1	timer flag active
Write	0	alarm flag is cleared	0	timer flag is cleared
	1	alarm flag remains unchanged	1	timer flag remains unchanged

Seconds,Minutes and Hours registers

Table 7 Seconds/VL register bits description(address 02H)

Bit	Symbol	Description
7	VL	VL = 0: reliable clock/calendar information is guaranteed; VL = 1: reliable clock/calendar information is no longer guaranteed.
6 to 0	<seconds>	These bits represent the current seconds value coded in BCD format; value = 00 to 59. Example: <seconds> = 101 1001, represents the value 59 s.

Table 8 Minutes register bits description(address 03H)

Bit	Symbol	Description
7	–	not implemented
6 to 0	<minutes>	These bits represent the current minutes value coded in BCD format; value = 00 to 59.

Table 9 Hours register bits description(address 04H)

Bit	Symbol	Description
7 to 6	–	not implemented
5 to 0	<hours>	These bits represent the current hours value coded in BCD format; value = 00 to 23.

Days,Weekdays,Months/Century and Years registers

Table 10 Days register bits description(address 05H)

Bit	Symbol	Description
7 to 6	–	not implemented
5 to 0	<days>	These bits represent the current day value coded in BCD format; value = 01 to 31. The BL5363 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year '00'.

Table 11 Weekdays register bits description(address 06H)

Bit	Symbol	Description
7 to 3	–	not implemented
2 to 0	<weekdays>	These bits represent the current weekday value 0 to 6; see Table 12. These bits may be re-assigned by the user.

Table 12 Weekday assignments

Day	Bit 2	Bit 1	Bit 0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 13 Months/Century register bits description(address 07H)

Bit	Symbol	Description
7	C	Century bit. C = 0; indicates the century is 20xx. C = 1; indicates the century is 19xx. 'xx' indicates the value held in the Years register; see Table 15. This bit is toggled when the Years register overflows from 99 to 00. These bits may be re-assigned by the user.
6 to 5	–	not implemented
4 to 0	<months>	These bits represents the current month value coded in BCD format; value = 01 to 12; see Table 14.

Table 14 Month assignments

Month	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Table 15 Years register bits description(address 08H)

Bit	Symbol	Description
7 to 0	<years>	This register represents the current year value coded in BCD format; value = 00 to 99.

Alarm registers

When one or more of the alarm registers are loaded with a valid minute, hour, day or weekday and its corresponding AE (Alarm Enable) bit is a logic 0, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the bit AF (Alarm Flag) is set.

AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE bit set at logic 1 will be ignored.

Table 16 Minute alarm register bits description(address 09H)

Bit	Symbol	Description
7	AE	AE = 0; minute alarm is enabled. AE = 1; minute alarm is disabled.
6 to 0	<minute alarm>	These bits represents the minute alarm information coded in BCD format; value = 00 to 59.

Table 17 Hour alarm register bits description(address 0AH)

Bit	Symbol	Description
7	AE	AE = 0; hour alarm is enabled. AE = 1; hour alarm is disabled.
6 to 0	<hour alarm>	These bits represents the hour alarm information coded in BCD format; value = 00 to 23.

Table 18 Day alarm register bits description(address 0BH)

Bit	Symbol	Description
7	AE	AE = 0; day alarm is enabled. AE = 1; day alarm is disabled.
6 to 0	<day alarm>	These bits represents the day alarm information coded in BCD format; value = 01 to 31.

Table 19 Weekday alarm register bits description(address 0CH)

Bit	Symbol	Description
7	AE	AE = 0; weekday alarm is enabled. AE = 1; weekday alarm is disabled.
6 to 0	<weekday alarm>	These bits represents the weekday alarm information value 0 to 6.

CLKOUT frequency register

Table 20 CLKOUT frequency register bits description(address 0DH)

Bit	Symbol	Description
7	FE	FE = 0; the CLKOUT output is inhibited and the CLKOUT output is set to high-impedance. FE = 1; the CLKOUT output is activated.
6 to 2	–	not implemented
1	FD1	These bits control the frequency output (f_{CLKOUT}) on the CLKOUT pin; see Table 21.
0	FD0	

Table 21 CLKOUT frequency selection

FD1	FD0	f_{CLKOUT}
0	0	32.768 kHz
0	1	1 024 Hz
1	0	32 Hz
1	1	1 Hz

Countdown timer registers

The Timer register is an 8-bit binary countdown timer. It is enabled and disabled via the Timer control register bit TE. The source clock for the timer is also selected by the Timer control register. Other timer properties, e.g. interrupt generation, are controlled via the Control/status 2 register. For accurate read back of the countdown value, the I^2C-bus clock SCL must be operating at a frequency of at least twice the selected timer clock.

Table 22 Timer control register bits description (address 0EH)

Bit	Symbol	Description
7	TE	TE = 0; timer is disabled. TE = 1; timer is enabled.
6 to 2	–	not implemented
1	TD1	Timer source clock frequency selection bits. These bits determine the source clock for the countdown timer, see Table 23. When not in use, TD1 and TD0 should be set to '11' ($1/60$ Hz) for power saving.
0	TD0	

Table 23 Timer source clock frequency selection

TD1	TD0	Timer source clock frequency (Hz)
0	0	4096
0	1	64
1	0	1
1	1	$1/60$

Table 24 Timer countdown value register bits description(address 0FH)

Bit	Symbol	Description
7 to 0	<timer countdown value>	This register holds the loaded countdown value 'n'. $\text{Countdown period} = \frac{n}{\text{Source clock frequency}}$

EXT_CLK test mode

A test mode is available which allows for on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in the Control/Status1 register. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with the signal that is applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT will then generate an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using the STOP bit. When the STOP bit is set, the pre-scaler is reset to 0. STOP must be cleared before the pre-scaler can operate again. From a STOP condition, the first 1 s increment will take place after32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 s increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

Operation example

1. Enter the EXT_CLK test mode; set bit 7 of Control/Status 1 register (TEST = 1)
2. Set bit 5 of Control/Status 1 register (STOP = 1)
3. Clear bit 5 of Control/Status 1 register (STOP = 0)
4. Set time registers (Seconds, Minutes, Hours, Days, Weekdays, Months/Century and Years) to desired value
5. Apply 32 clock pulses to CLKOUT
6. Read time registers to see the first change
7. Apply 64 clock pulses to CLKOUT
8. Read time registers to see the second change.

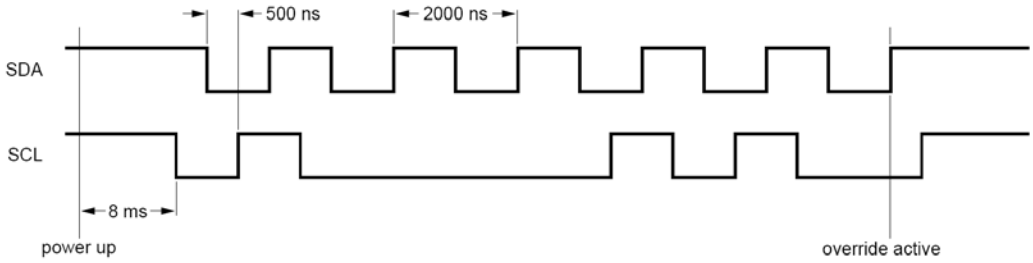
Repeat steps 7 and 8 for additional increments.

Power-On Reset (POR) override mode

The POR duration is directly related to the crystal oscillator start-up time. Due to the long

start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I^2C-bus pins, SDA and SCL, be toggled in a specific order as shown in Figure 5. All timing values are required minimum.

Once the override mode has been entered, the chip immediately stops being reset and normal operation starts i.e. entry into the EXT_CLK test mode via I^2C-bus access. The override mode is cleared by writing a logic 0 to bit TESTC. Re-entry into the override mode is only possible after TESTC is set to logic 1. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.



POR override sequence

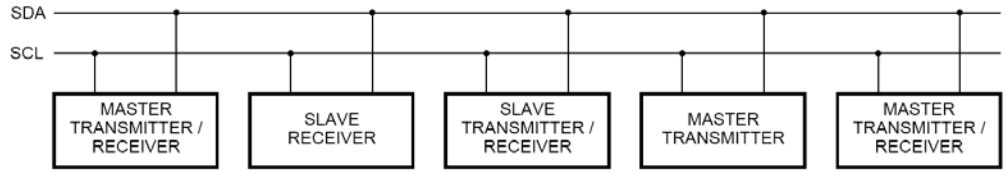
Serial interface

The serial interface of the BL5363 is the I^2C-bus. A detailed description of the I^2C-bus specification, including applications, is given in the brochure: The I^2C-bus and how to use it, order no. 9398 393 40011 or I^2C Peripherals Data Handbook IC12.

Characteristics of the I^2C-bus

The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

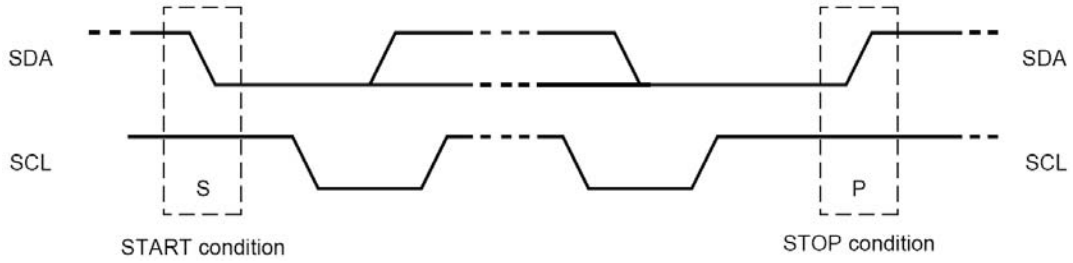
The I^2C-bus system configuration is shown in Figure below. A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.



I^2C-bus system configuration

START and STOP conditions

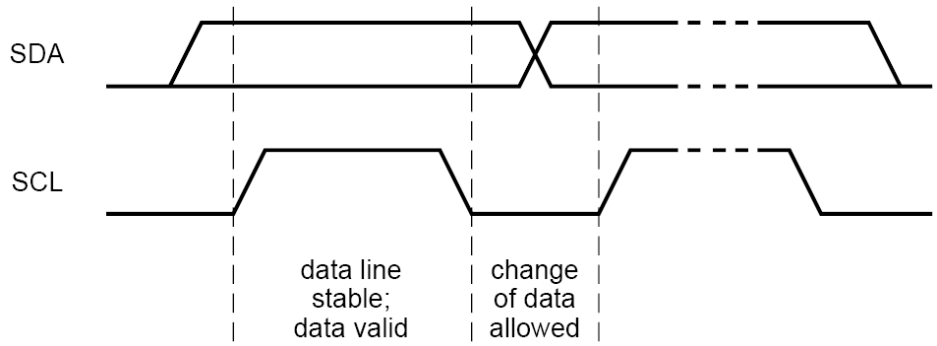
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P); see Figure below.



START and STOP conditions I^2C-bus

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure below..



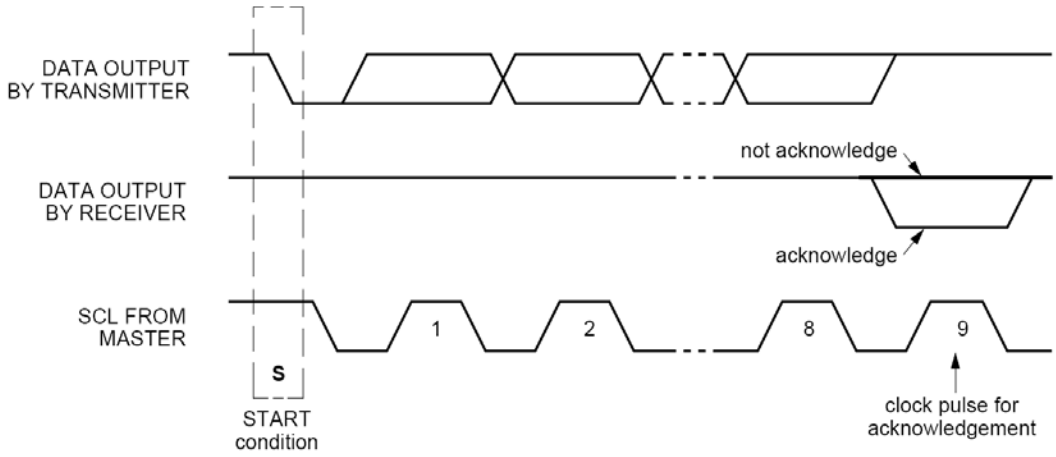
Bit transfer on the I^2C-bus

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

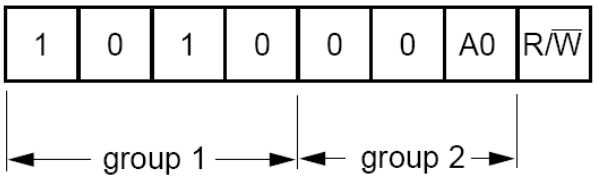
The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



Acknowledge on the I^2C-bus

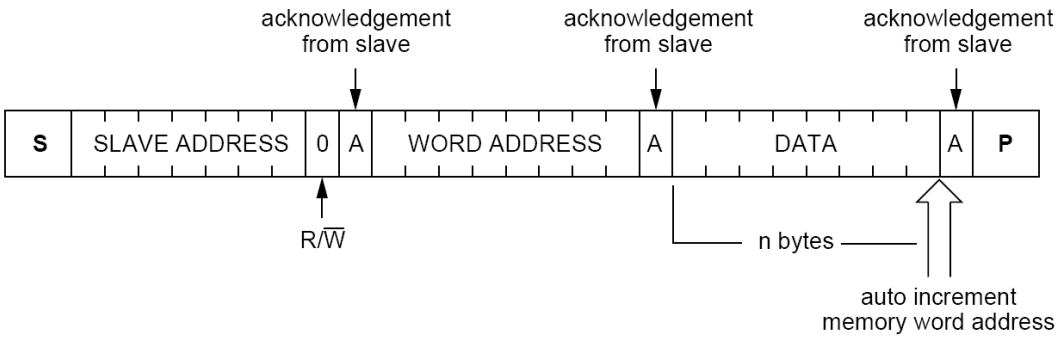
I^2C-bus protocol

Addressing: Before any data is transmitted on the I2C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.
The BL5363 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.
The BL5363 slave address is shown in Figure below.

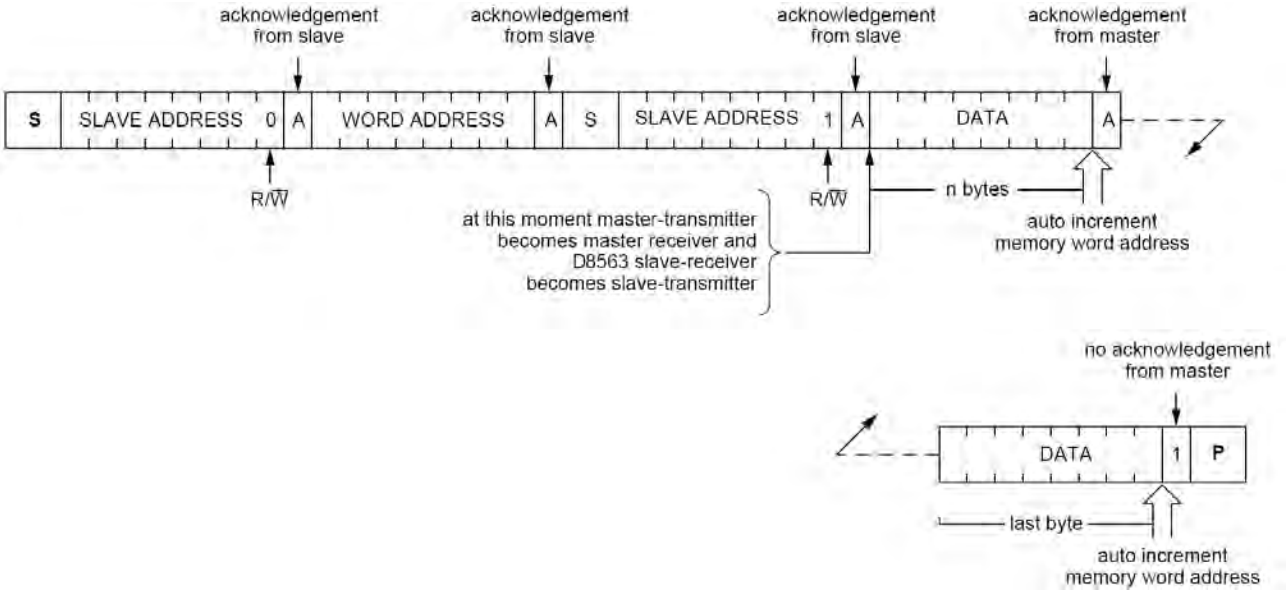


Slave address

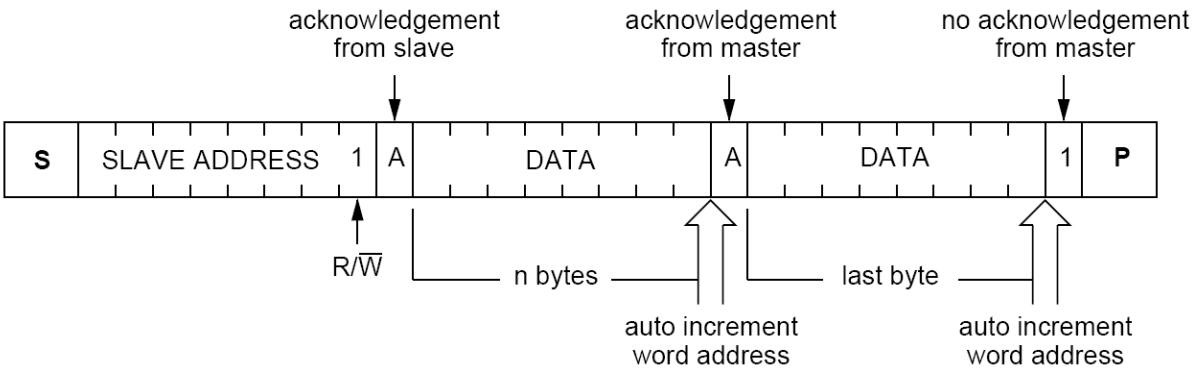
Clock/calendar read/write cycles: The I^2C-bus configuration for the different BL5363 read and write cycles are shown in Figure 11, 12 and 13. The word address is a four bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.



Master transmits to slave receiver(write mode)

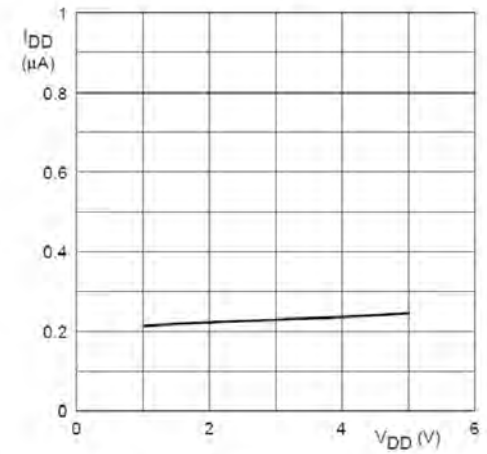


Master reads affer setting word address(write word address;read data)



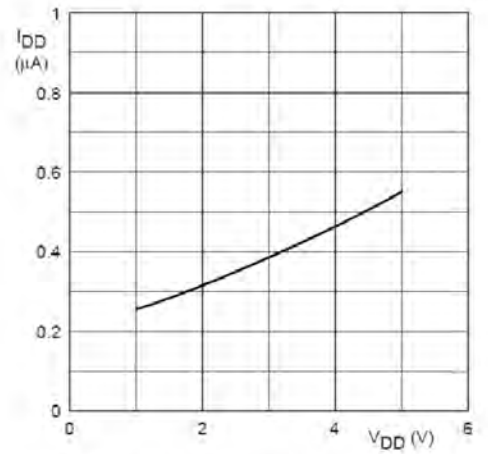
Master reads slave immediately after first byte (read mode)

CHARACTERISTICS CURVES



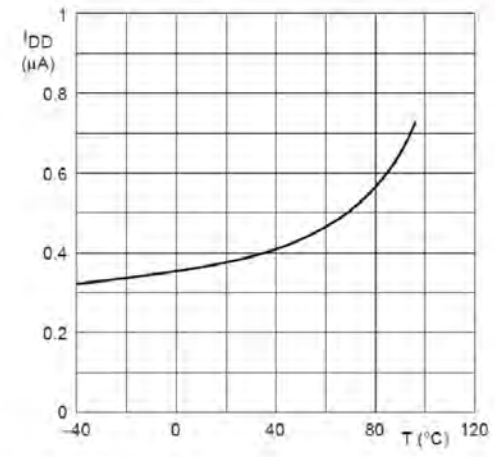
T_{amb} = 25 °C; Timer = 1 minute.

I_{DD} as a function of V_{DD}; CLKOUT disabled.



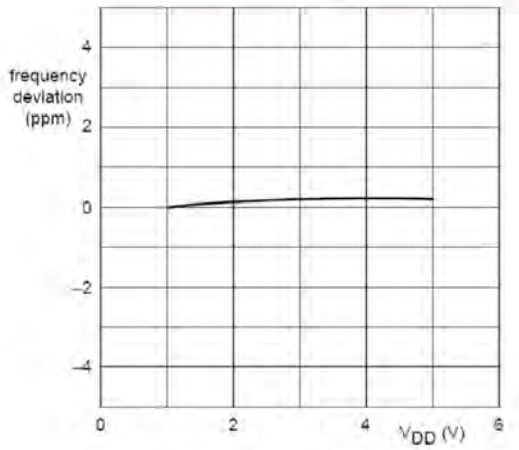
T_{amb} = 25 °C; Timer = 1 minute.

I_{DD} as a function of V_{DD}; CLKOUT = 32 kHz.



V_{DD} = 3 V; Timer = 1 minute.

I_{DD} as a function of T_{amb}; CLKOUT = 32 kHz.

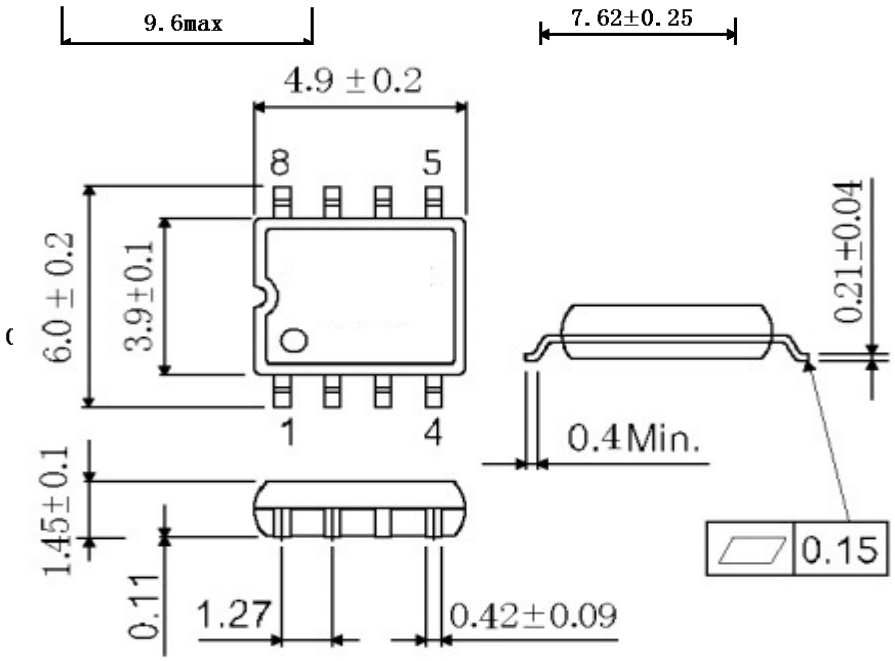


T_{amb} = 25 °C; normalized to V_{DD} = 3 V.

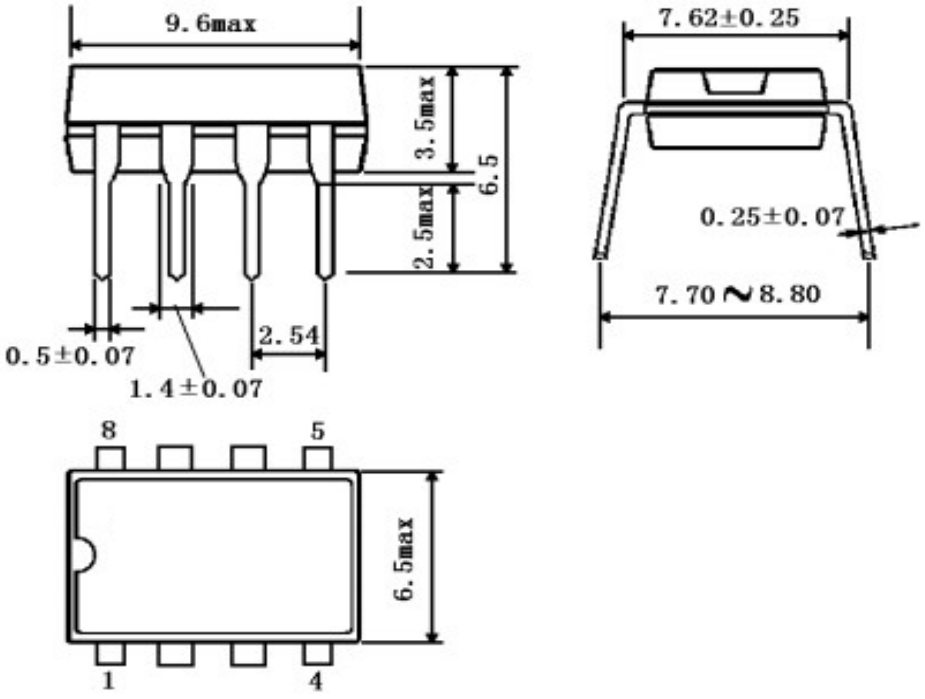
Frequency deviation as function of V_{DD}.

OUTLINE DRAWING

DIP8 Unit:mm



SOP8 Unit:mm



TSSOP8 Unit:mm