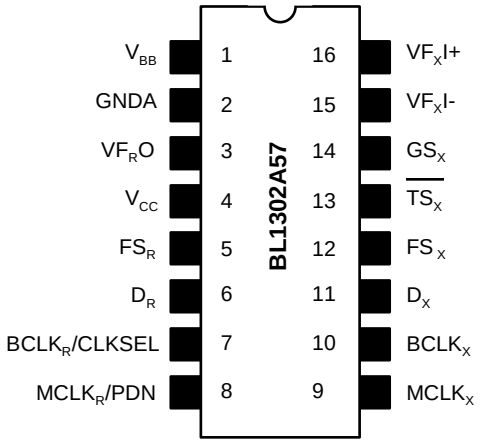
General Description

The BL1302A57/S is an A-law monolithic PCM CODEC/filter which has the A/D and D/A conversion and a serial PCM interface. The device is fabricated using the advanced double-poly nwell CMOS process. It is pin compatible with TP3057.

The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law PCM format. The decode portion consists of an expanding decoder, which reconstructs the Analog signal from the companded A-law code, a low-pass filter which corrects for the sinx/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The device requires two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks , which may vary from 64 KHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Pin Assignment



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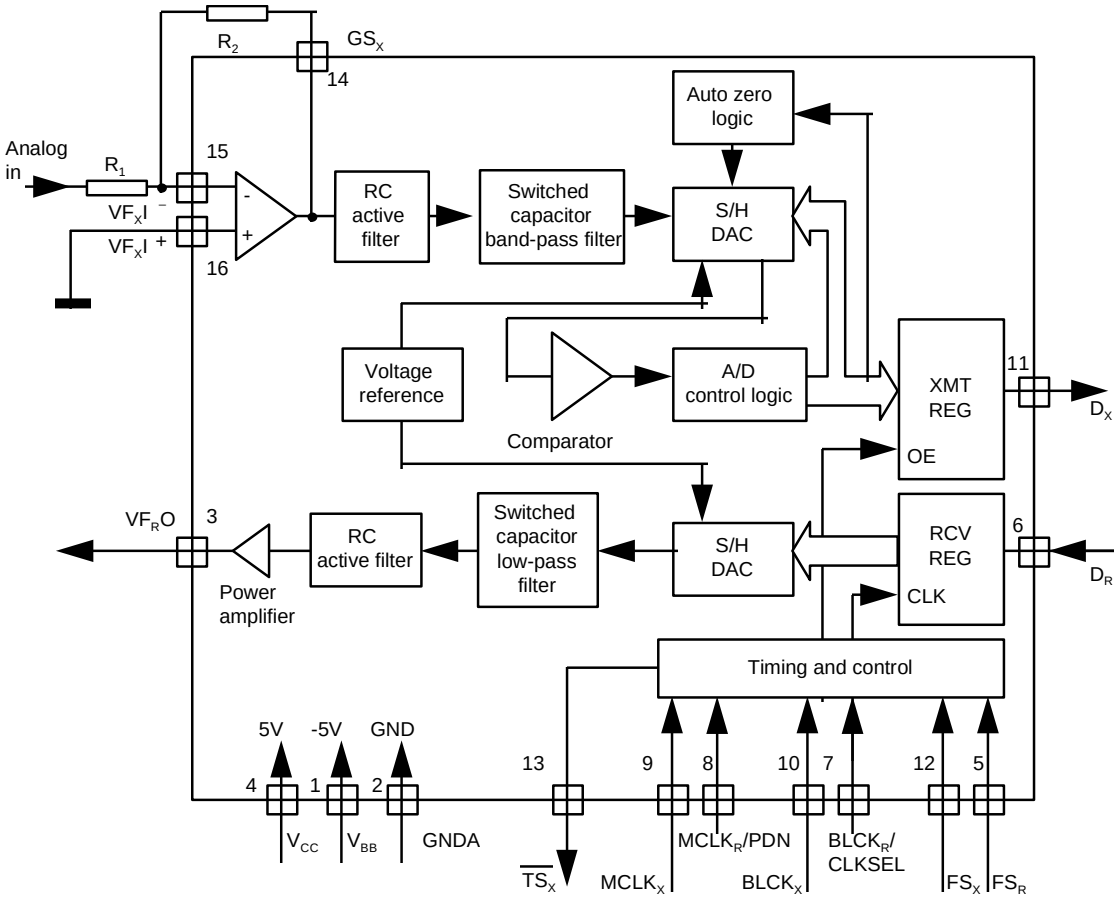
Features

- Complete CODEC and filtering system (COMBO) including:
  - --- Transmit high-pass and low-pass filtering
  - --- Receive low-pass filter with sinx/x correction
  - --- Active RC noise filters
  - --- A-law compatible COder and DECoder
  - --- Internal precision voltage reference
  - --- Serial I/O interface
  - --- Internal auto-zero circuitry
- 16 pin DIP or SOP
- Designed for ITU application

- ±5V operation
- Low power: Typical 50mW
  Stand-by 3mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces

Block Diagram



Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. V_{BB}= - 5V ±5%
GNDA	Analog ground. All signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier.
V_{CC}	Positive power supply pin. Vcc= +5V±5%
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R.FS_R is an 8kHz pulse train.
D_R	Receive data input. PCM data is shifted into D_R following the FSR leading edge.
$BLCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64kHz to 2.048 MHz. Alternatively , may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and BCLKx is used for both transmit and receive directions(see Table 1).
$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. In synchronous mode, it may be needed as a power-down control. When $MCLK_R$ is connected continuously low, MCLKx is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
MCLKx	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. In synchronous mode, it is also used as receive master clock.
FSx	Transmit frame sync pulse input which enables BCLKx to shift out the PCM data on Dx. FSx is an 8 KHz pulse train.
BCLKx	The bit clock which shifts out the PCM data on Dx. May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLKx.
Dx	The TRI-STATE PCM data output which is enabled by FSx.
$\overline{TSx}$	Open drain output which pulses low during the encoder time slot.
GSx	Analog output of the transmit input amplifier. Used to externally set gain.
VFx I-	Inverting input of the transmit input amplifier.
VFx I+	Non-inverting input of the transmit input amplifier.

Functional Description

- **Power-up**

When power is first applied, the internal power-on reset circuitry initializes the device and places it into a power-down state. Most of the analog and digital circuits are deactivated, and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FSx and/or FS_R pulses must be present.

Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R input continuously low---the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FSx or FS_R pulse. The TRI-STATE PCM data output, Dx, will remain in the high impedance state until the second FSx pulse.

- **Synchronous operation**

For synchronous operation, the same master clock should be used for both the transmit and receive directions. In this mode , a clock must be applied to MCLKx and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, MCLKx will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to BCLKx and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, BCLKx will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL . In this synchronous mode, the bit clock, BCLKx and $BCLK_R$, may be from 64kHz to 2.048 MHz. The frequency of BCLKx and $BCLK_R$ are not necessary to be equal, but must be synchronous with MCLKx.

Each FSx pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled Dx output on the positive edge of BCLKx. After 8 bit clock periods, the TRI-STATE Dx output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of BCLKx (or BCLKR if running). FSx and FS_R must be synchronous with $MCLK_X$/$_R$.

Table Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected
Clocked	2.048MHz
0	1.536MHz or 1.544MHz
1	2.048MHz

- **Short frame operation**

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, frame sync pulse, FSx and FS_R , must be one bit clock period long, with timing relationships specified in Figure 1. With FSx high during a falling edge of BCLKx, the next rising edge of BCLKx enables the Dx TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the Dx output. With FS_R high during a falling edge of $BCLK_R$ (BCLKx, if $BCLK_R$ is a fixed level), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

- **Long frame operation**

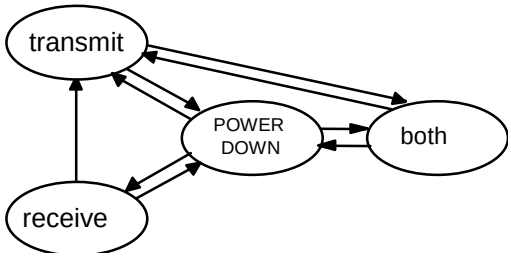
To use the long frame mode, the frame sync pulse, FSx and FS_R , must be three or more bit clock periods long, with timing relationships specified in Figure 2. Based on the transmit frame sync, FSx, the device will sense whether short or long frame sync pulse are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160ns. The Dx tri-state output buffer is enabled with the rising edge of FSx or the rising edge of BCLKx , whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLKx rising edges clock out the remaining seven bits. The Dx output is disabled by the falling BCLKx edge following the eighth rising edge, or by FSx going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ (BCLKx if $BCLK_R$ is a fixed level).

- **Single channel operation**

Keeping FS_R input continuously low, the device enters into transmit channel operation, the data at D_R input will be ignored. Keeping FS_X input continuously low, the device enters into receive channel operation. The most part of transmit circuitry ceases to work, D_X and TS_X output will be in high impedance. If $MCLK_R$ input is a clock, it is the internal master clock. If $MCLK_R$ input is not a clock, $MCLK_X$ is the internal master clock, and $MCLK_X$ must be synchronous with FS_R. If $BCLK_R$ input is not a clock, $BCLK_X$ is the internal bit clock. In receive channel operation, the length of FS_R determines whether it is short or long frame.

- **Switch of operation**

See picture below, it is not recommended that the switching from both channels to receive only or switching from receive channel only to transmit channel only.



- **Transmit section**

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law coding conventions. A built-in bandgap voltage reference is used to provide an input overload of nominally 2.492V peak. The FSx frame pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through Dx at the next FSx pulse. The total encoding delay will be approximately 165us (due to transmit filter) plus 125us (due to encoding delay), which totals 290us. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

- **Receive section**

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law and the 5th order low pass filter corrects for the sinx/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600ohm load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ (BCLKx) periods. At the end of the decoder time slot, the decoding cycle begins. The total decoder delay approximately 280 us.

Electrical parameters and timing

Absolute Maximum Ratings

Rating	Value	Unit
V_{CC} to GNDA	7	V
V_{BB} to GNDA	-7	V
Voltage at any Analog Input or Output	VCC+0.3 to VBB-0.3	V
Voltage at any Digital Input or Output	VCC+0.3 to GNDA-0.3	°C
Operating Temperature Range	-25 to +125	°C
Storage Temperature Range	-65 to +150	°C
ESD (Human Body Model)	1000	V
Latch-Up Immunity at any Pins	100	mA

Electrical Characteristics: V_{CC} = +5.0V±5%, V_{BB} = -5.0V±5%, T_A = 0°C to +70°C. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = -5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	Dx, I_L=3.2mA TSx, I_L=3.2mA, Open Drain			0.4 0.4	V V
V_{OH}	Output High Voltage	Dx, I_H= - 3.2mA	2.4			V
I_{IL}	Input Low Current	GNDA≤V_{IN}≤V_{IL},All digital inputs	-10		10	μA
I_{IH}	Input High Current	V_{IH}≤V_{IN}≤Vcc	-10		10	μA
IOZ	Output Current in High Impedance State (TRI-STATE)	Dx, GNDA≤V_O≤Vcc	-10		10	μA

Ananalog Interface with transmit input amplifier						
I_IXA	Input Leakage Current	-2.5V≤V≤+2.5V, VFxI+ or VFxI-	-200		200	nA
R_IXA	Input Resistance	-2.5V≤V≤+2.5V, VFxI+ or VFxI-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GSx	10			kΩ
C_LXA	Load Capacitance	GSx			50	pF
V_OXA	Output Dynamic Range	GSx, R_L ≥10kΩ	-2.8		2.8	V
A_VXA	Voltage Gain	VFxI+ to GSx	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
V_{OS}XA	Offset Voltage		-20		20	mV
V_{CM}XA	Common-Mode Voltage	CMRRXA>60dB	-2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	60			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO=±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		-200		200	mV
POWER DISSIPATION						
$I_{CC}0$	Power-Down Current	No Load (Note)		0.14	0.3	mA
$I_{BB}0$	Power-Down Current	No Load(Note)		0.20	1.5	mA
$I_{CC}1$	Power-Up Active Current	No Load		5.0	10	mA
$I_{BB}1$	Power-Up Active Current	No Load		5.0	10	mA

Note: Icc0 and $I_{BB}0$ are measured after first achieving a power-up state.

Timing Specifications: V_{CC} =+5.0±5%, V_{BB} = -5.0±5%, Ta = 0°C ~+70 °C. All signals referenced to GNDA. Typicals specified at V_{OH} =+5.0V, V_{BB} = -5.0V, T_H = 25°C. All timing parameters are assured at V_{OH} =2.0V and V_{OL} = 0.7V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	Depends on		1.536		MHz

		$BCLK_R$/CLKSEL Pin. MCLKx and $MCLK_R$		1.544 2.048		MHz MHz
t_{RM}	Rise Time of Master Clock	MCLKx and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	MCLKx and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock		485	488	15725	ns
t_{RB}	Rise Time of Bit Clock	BCLKx and $BCLK_R$			50	ns
t_{FB}	Fall Time of Bit Clock	BCLKx and $BCLK_R$			50	ns
t_{WMH}	Width of Master Clock High	MCLKx and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	MCLKx and $MCLK_R$	160			ns
t_{SBFM}	Set-Up Time from BCLKx High to MCLKx Falling Edge	First Bit Clock after the Leading Edge of FSx	100			ns
t_{SFFM}	Set-up Time from FSx High to MCLKx Falling Edge	Long Frame Only	100			ns
t_{WBH}	Width of Bit Clock High	VIH=2.2V	160			ns
t_{WBL}	Width of Bit Clock Low	VIL=0.6V	160			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from BCLKx High to Data Valid	Load=150 pF plus 2 LSTTL	0		140	ns
t_{DBTS}	Delay Time to TSx Low	Load=150 pF plus 2 LSTTL Loads	0		140	ns
t_{DZC}	Delay Time from BCLKx Low to Data Output Disabled	CL=0 pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FSx or BCLKx, Whichever Comes Later	CL=0 pF to 150 pF	20		165	ns
t_{SDB}	Set-Up time from D_R Valid to $BCLK_R$/X Low		50			ns
t_{HBD}	Hold Time from $BCLK_R$/X Low to D_R Invalid		50			ns
t_{SF}	Set-Up Time from FS_X/R to	Short Frame Sync Pulse	50			ns

	BCLK $_{X/R}$ Low	(1 Bit Clock Period Long)				
t_{HF}	Hold Time from BCLK$_{X/R}$ Low to FS $_{X/R}$ Low	Short Frame Sync Pulse (1 bit Clock Period Long)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FSx or FS $_{R}$)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160			ns

Timing diagrams

Figure 1. Short Frame Sync Timing

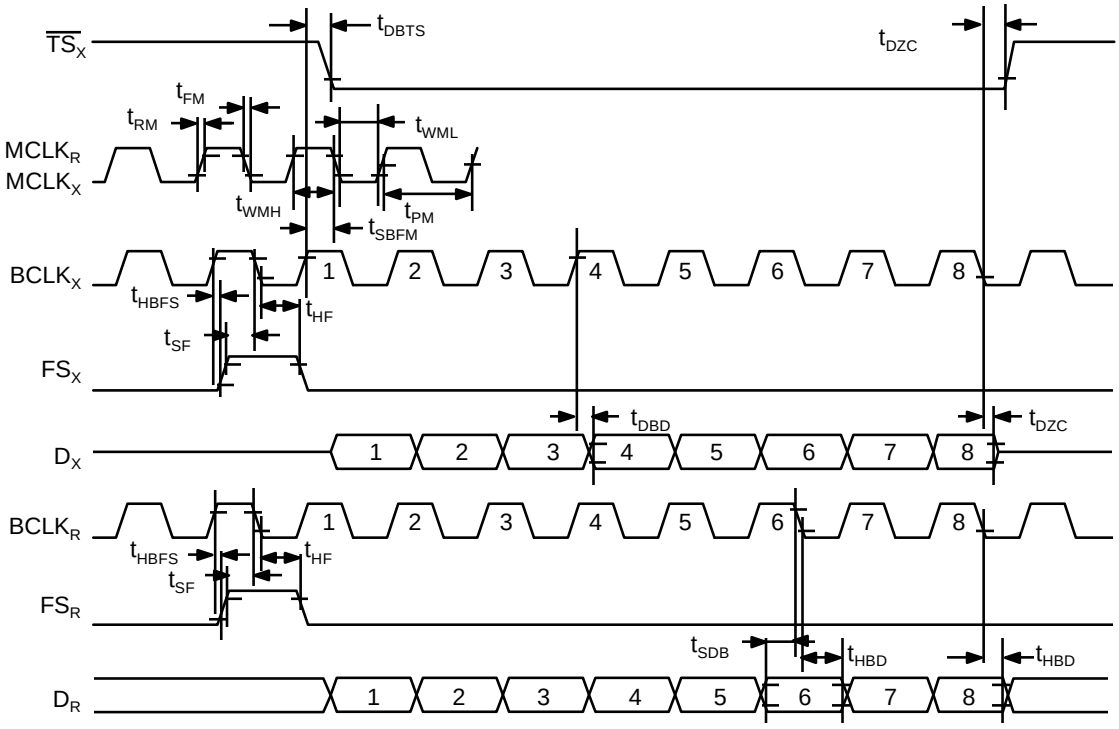
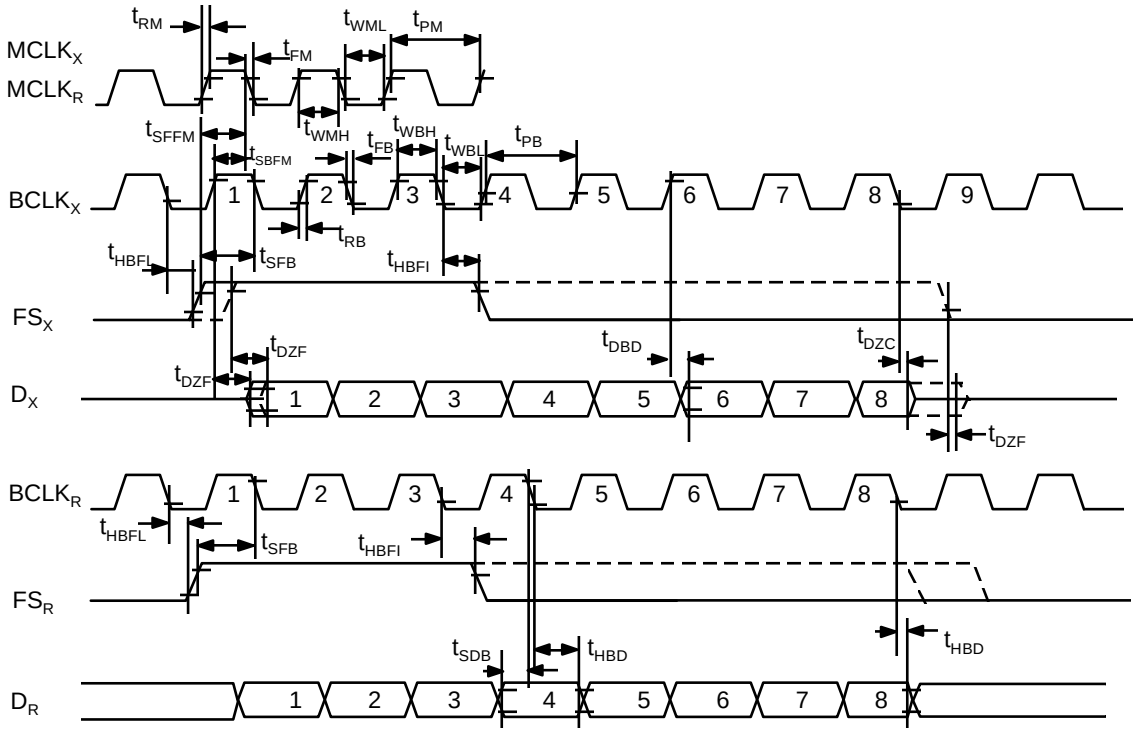


Figure 2. Long Frame Sync Timing



Transmission Characteristics: V_{CC} = +5.0V±5%, V_{BB} = -5.0V±5%, GNDA=0V,T_A = 0°C to +70 °C, f=1.02kHz, Vin=0dBm0, transmit input amplifier connected for unity gain inverting. Typicals are specified at V_{CC} = +5V, V_{BB} = -5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Amplitude resopnse						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm(600Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Virtual Decision Valve Defined Per CCITT Rec. G711	Max Overload Level (3.14 dBm0)		2.492		V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25 ^{0}C,Vcc=5V, V_{BB}= -5V Input at Gsx=0 dBm0 at 1020 Hz	-0.25		0.25	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16Hz f=50Hz f=60Hz f=200Hz	 -1.8	 	-40 -30 -26 -0.1	dB dB dB dB

		f=300Hz-3000Hz f=3300Hz f=3400Hz f=4000Hz f=4600Hz and Up, Measure Response from 0 Hz to 4000 Hz	-0.15 -0.35 -0.7		0.15 0.05 0 -14 -32	dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	-0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	-0.05		0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level=-10dBm0 VFxI+=-40dBm0 to +3dBm0 VFxI+=-50dBm0 to-40dBm0 VFxI+=-55dBm0 to-50dBm0	 -0.2 -0.4 -1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A=25 ^{0}C,Vcc=5V,V_{BB}=-5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	-0.25		0.25	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0Hz to 3000 Hz f=3300Hz f=3400Hz f=4000Hz	-0.15 -0.35 -0.7		0.15 0.05 0 -14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	-0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	-0.05		0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level				

		=-40 dBm0 to +3 dBm0	-0.2		0.2	dB
		=-50 dBm0 to -40 dBm0	-0.4		0.4	dB
		=-55 dBm0 to -50 dBm0	-1.2		1.2	dB
V_{RO}	Receive Output Drive Level	R_L=600Ω	-2.5		2.5	V
Envelope delay distortion with frequency						
D_{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	us
Dx_R	Transmit Delay, Relative to D_{XA}	f=500 Hz - 600 Hz		195	220	us
		f=600 Hz - 800 Hz		120	145	us
		f=800 Hz - 1000 Hz		50	75	us
		f=1000 Hz - 1600 Hz		20	40	us
		f=1600 Hz - 2600 Hz		55	75	us
		f=2600 Hz - 2800 Hz		80	105	us
		f=2800 Hz - 3000 Hz		130	155	us
D_{RA}	Receive Delay, Absolute	f=1600 Hz		270	290	us
D_{RR}	Receive Delay, Relative to D_{RA}	f=500 Hz - 1000 Hz	-40	-25		us
		f=1000 Hz - 1600 Hz	-30	-20		us
		f=1600 Hz - 2600 Hz		70	90	us
		f=2600 Hz - 2800 Hz		100	125	us
		f=2800 Hz - 3000 Hz		145	175	us
Noise						
N_{XP}	Transmit Noise, P Message Weighted			-74	-67	dBm0p
N_{RP}	Receive Noise, P Message Weighted	PCM Code Equals Positive Zero		-82	-79	dBm0p
N_{RS}	Noise, Single Frequency	f=0kHz to 100 kHz, Loop Around Measurement, VFxI+=0 Vrms			-53	dBm0
PPSRx	Positive Power Supply Rejection, Transmit	VFxI+= -50 dBm0 Vcc=5.0 V_{DC}+100 mVrms f=0 kHz - 50 kHz (Note 2)	40			dBC
NPSRx	Negative Power Supply Rejection, Transmit	VFxl+= -50 dBm0 Vcc=-5.0 V_{DC}+100 mVrms f=0 kHz - 50 kHz (Note 2)	40			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero,Vcc=5.0V_{DC}+100mVrms Measure VF_RO				

		f=0 Hz - 4000 Hz f=4 kHz - 25 kHz f=25 kHz - 50 kHz	40 40 36			dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM code Equals Positive Zero,V_{BB}=-5.0V_{DC}+100mVrms Measure VF_RO f=0 Hz - 4000 Hz f=4 kHz - 25 kHz f=25 kHz - 50 kHz	 40 40 36			 dBC dB dB
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R. 4600 Hz - 7600 Hz 7600 Hz - 8400 Hz 8400 Hz - 100,000 Hz			 -30 -40 -30	 dB dB dB
Distortion						
STDx STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3) Level=3.0 dBm0 =0 dBm0 to - 30 dBm0 =-40 dBm0 XMT RCV =-55 dBm0 XMT RCV	 33 36 29 30 14 15			 dBC dBC dBC dBC dBC dBC
SFDx	Single Frequency Distor-tion, Transmit				-46	dB
SFD_R	Single frequency Distor-tion, Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VFx+=-4dBm0 to -21 dBm0, Two Frequencies in the			-41	dB

		Range 300 Hz-3400Hz				
Crosstalk						
$CTx\text{-}_R$	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f=300Hz-3400Hz D_R=Quiet PCM Code (Note 2)		-90	-75	dB
$CT_R\text{-}x$	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f=300Hz-3400Hz, VFxI=Multitone (Note1)		-90	-70	dB

Note 1: Measured by extrapolation from the distortion test result at -50 dBm0.

Note 2: PPSRx, NPSRx, and CTR-X are measured with a -50 dBm0 activation signal applied to VFxl+ .

Note 3: Device is measured using psophometric-weighted filter.

Encoding Format at Dx Output

Vin (at GSx) = +Full-Scale	1 0 1 0 1 0 1 0
Vin (at GSx) = 0V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
Vin (at GSx) = -Full-Scale	0 0 1 0 1 0 1 0

Applications Information

Power supplies

While the pins of the device are well protected against electrical misuse, it is recommended that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a “hot” socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to Vcc and V_{BB}, as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

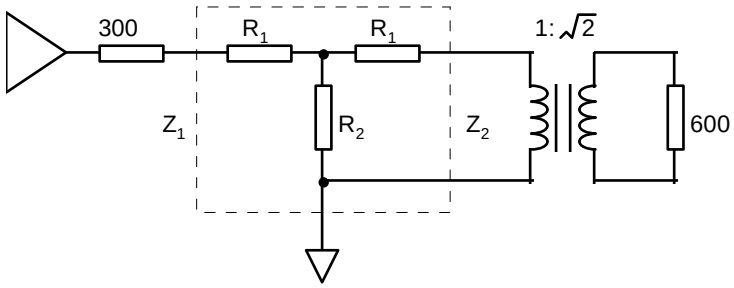
This common ground point should be decoupled to Vcc and V_{BB} with 10μF capacitors.

Receive gain adjustment

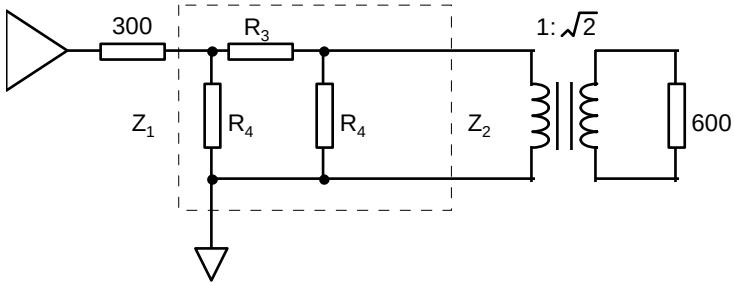
For applications where a device CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. The followed table lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss.

Attenuator diagram and table

T-Pad attenuator



π - Pad attenuator



Where

$$R_1 = Z_1\frac{N^2+1}{N^2-1} - 2\sqrt{Z_1 Z_2}\bullet\frac{N}{N^2-1}$$

$$R_2 = 2\sqrt{Z_1 Z_2}\bullet\frac{N}{N^2-1}$$

$$R_3 = \sqrt{\frac{Z_1 Z_2}{2}}\bullet\left(\frac{N^2-1}{N}\right)$$

$$R_4 = Z_1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

$$N = \sqrt{\frac{Power\ in}{Power\ out}}$$

$$S = \sqrt{\frac{Z_1}{Z_2}}$$

$$Z = \sqrt{Z_{SC}\bullet Z_{OC}}$$

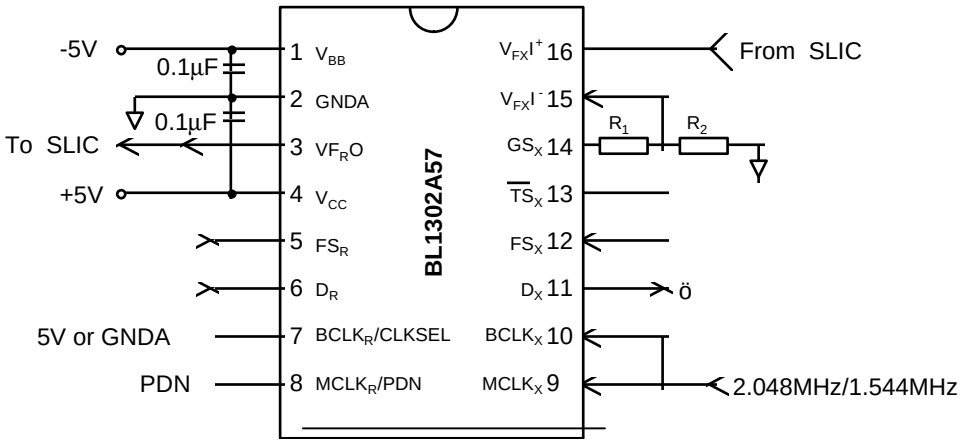
Z_{SC} = inpedance with short circuit termination

Z_{OC} = inpedance with open circuit termination

Attenuator Table for $Z_1=Z_2=300W$, all values in W

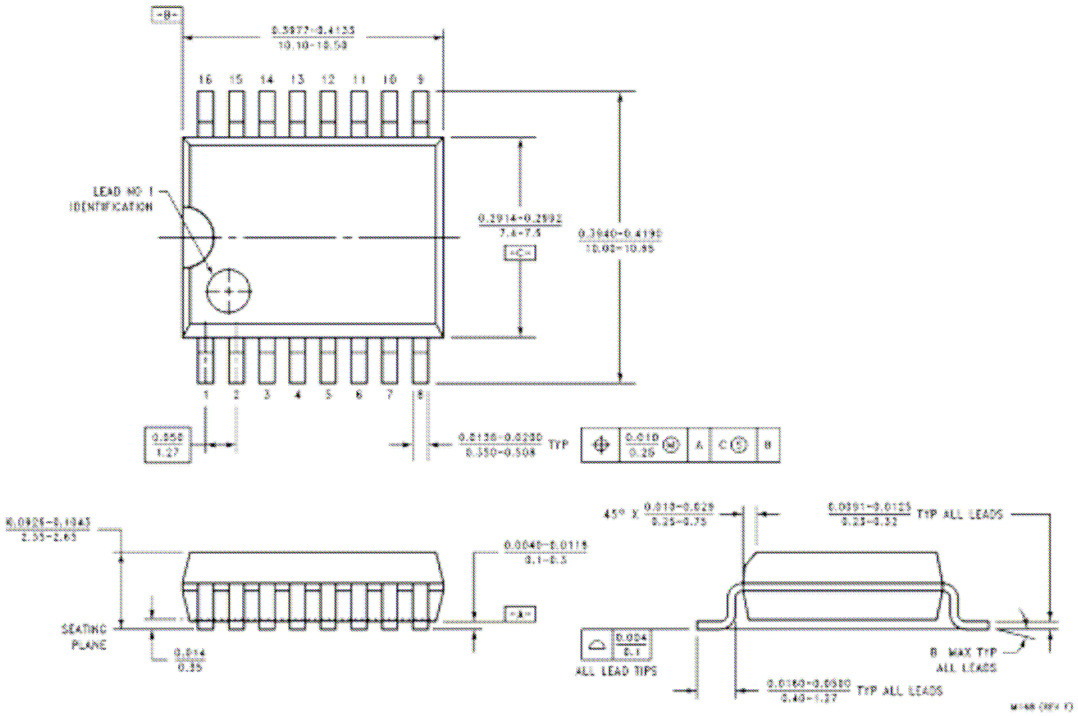
dB	R_1	R_2	R_3	R_4	dB	R_1	R_2	R_3	R_4
0.1	1.7	26k	3.5	52k	6	100	402	224	900
0.2	3.5	13k	6.9	26k	7	115	380	269	785
0.3	5.2	8.7k	10.4	17.4k	8	379	284	317	698
0.4	6.9	6.5k	13.8	13k	9	143	244	370	630
0.5	8.5	5.2k	17.3	10.5k	10	156	211	427	527
0.6	10.4	4.4k	21.3	8.7k	11	168	184	490	535
0.7	12.1	3.7k	24.2	7.5k	12	180	161	550	500
0.8	13.8	3.3k	27.7	6.5k	13	190	142	635	473
0.9	15.5	2.9k	31.1	5.8k	14	200	125	720	450
1.0	17.3	2.6k	34.6	5.2k	15	210	110	816	430
2	34.4	1.3k	70	2.6k	16	218	98	924	413
3	51.3	850	107	1.8k	18	233	77	1.17k	386
4	68	650	144	1.3k	20	246	61	1.5k	366
5	84	494	183	1.1k					

Typical synchronous application

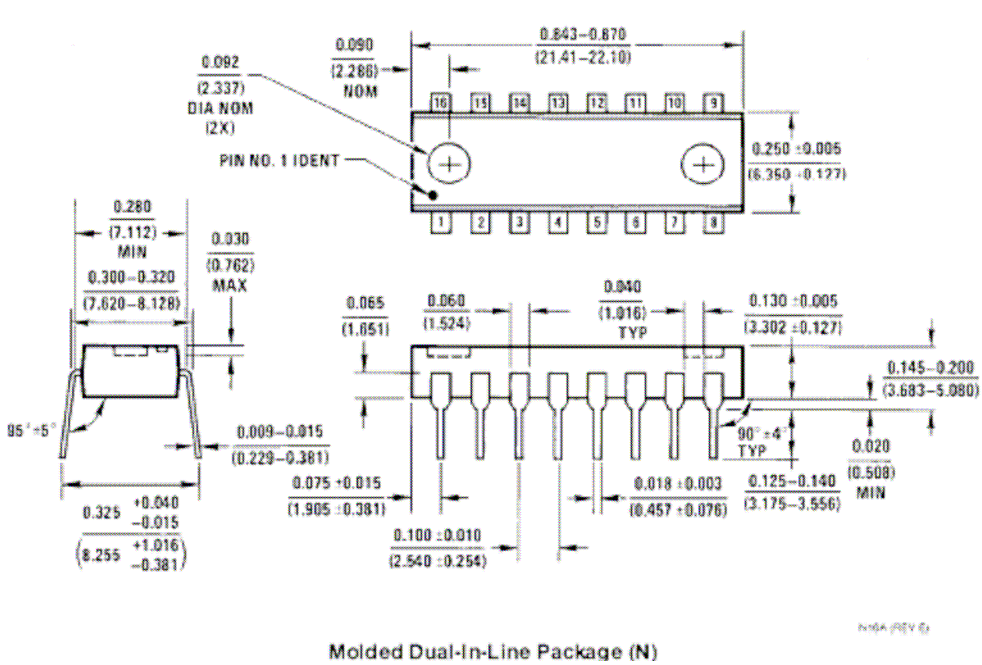


Print Information

Physical Dimensions inches (millimeters)



Molded Small Outline Package (WM)



Molded Dual-In-Line Package (N)