



U74AHC1G02

CMOS IC

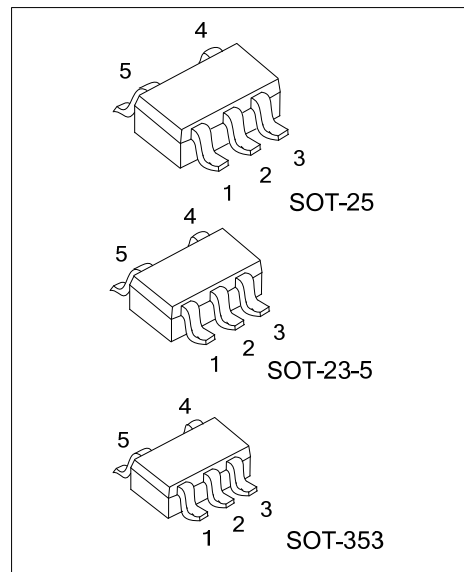
2-INPUT NOR GATE

DESCRIPTION

The U74AHC1G02 is a single 2-input NOR gate which provides the Function $Y=A+B$.

FEATURES

- * Operation Voltage Range: 2.0~5.5V
- * Low Power Dissipation
- * High noise immunity
- * Balanced propagation delays
- * Specified from -40 to +125°C

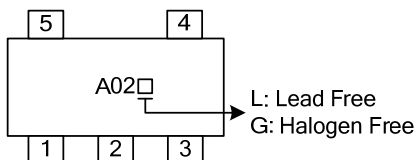


ORDERING INFORMATION

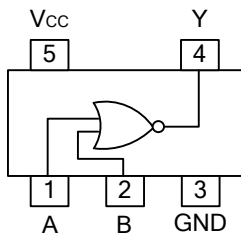
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC1G02L-AE5-R	U74AHC1G02G-AE5-R	SOT-23-5	Tape Reel
U74AHC1G02L-AF5-R	U74AHC1G02G-AF5-R	SOT-25	Tape Reel
U74AHC1G02L-AL5-R	U74AHC1G02G-AL5-R	SOT-353	Tape Reel

<p>U74AHC1G02L-AE5-R</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) R: Tape Reel (2) AE5: SOT-23-5, AF5: SOT-25, AL5: SOT-353 (3) L: Lead Free, G: Halogen Free</p>
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MARKING



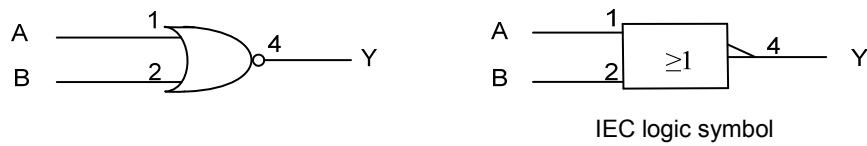
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Voltage	V_{IN}	-0.5~7	V
Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Continuous Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0	5.0	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Times	t_R, t_F	$V_{CC}=3.3V\pm0.3V$			100	ns/V
		$V_{CC}=5V\pm0.5V$			20	
Operating Temperature	T_A		-40	25	125	°C

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5			V
		$V_{CC}=3.0V$	2.1			
		$V_{CC}=5.5V$	3.85			
Low-Level Input Voltage	V_{IL}	$V_{CC}=2.0V$			0.5	V
		$V_{CC}=3.0V$			0.9	
		$V_{CC}=5.5V$			1.65	
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V, I_{OH}=-50\mu A$	1.9	2.0		V
		$V_{CC}=3.0V, I_{OH}=-50\mu A$	2.9	3.0		
		$V_{CC}=4.5V, I_{OH}=-50\mu A$	4.4	4.5		
		$V_{CC}=3.0V, I_{OH}=-4mA$	2.58			
		$V_{CC}=4.5V, I_{OH}=-8mA$	3.94			
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V, I_{OL}=50\mu A$			0.1	V
		$V_{CC}=3.0V, I_{OL}=50\mu A$			0.1	
		$V_{CC}=4.5V, I_{OL}=50\mu A$			0.1	
		$V_{CC}=3.0V, I_{OH}=4mA$			0.36	
		$V_{CC}=4.5V, I_{OH}=8mA$			0.36	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0V\sim5.5V, V_{IN}=V_{CC}$ or GND			±0.1	μA
Quiescent Supply Current	I_Q	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			1	μA
Input Capacitance	C_{IN}	$V_{CC}=5V, V_{IN}=V_{CC}$ or GND		4	10	pF

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

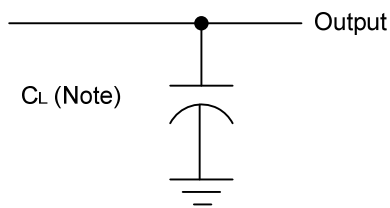
■ SWITCHING CHARACTERISTICS (Input signal: $T_A = 25^\circ\text{C}$, $\text{PRR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_R \leq 3\text{ns}$, $t_F \leq 3\text{ns}$.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Times	t_{PLH}	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $C_L = 15\text{pF}$		5.6	7.9	ns
		$V_{CC} = 5\text{V} \pm 0.5\text{V}$, $C_L = 15\text{pF}$		3.6	5.5	
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $C_L = 50\text{pF}$		8.1	11.4	
		$V_{CC} = 5\text{V} \pm 0.5\text{V}$, $C_L = 50\text{pF}$		5.1	7.5	
	t_{PHL}	$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $C_L = 15\text{pF}$		5.6	7.9	ns
		$V_{CC} = 5\text{V} \pm 0.5\text{V}$, $C_L = 15\text{pF}$		3.6	5.5	
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $C_L = 50\text{pF}$		8.1	11.4	
		$V_{CC} = 5\text{V} \pm 0.5\text{V}$, $C_L = 50\text{pF}$		5.1	7.5	

■ OPERATING CHARACTERISTIC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load, $f = 1\text{MHz}$, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$		15		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: CL includes probe and jig capacitance.

Fig.1 Load circuitry for switching times.

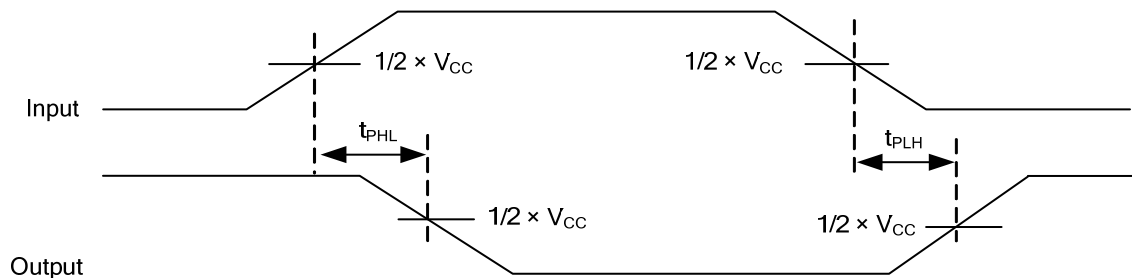


Fig.2 Propagation delay from input(A and B) to output(Y)

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